

Monolithic Pixels for ILC at LBNL From Sensor R&D to Simulation Studies

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LBNL LDRD-Chip 1



LDRD-Chi p 1: first test structure developed at LBNL, part of ongoing LDRD pixel project for the ILC: simple 3T pixels, analog output, 3 matrices with 10x10 μ m², 20x20 μ m² and 40x40 μ m² pixels;

Produced in Spring 05 in AMS 0. 35-OPTO process, estimated 10 µm epi-layer;

Simple structure useful for comparing response of different pixel geometries.

LDRD-1 Chip: 200 keV e⁻ Microscope Test

Test at the JEOL 200CX TEM electron microscope at LBNL NCEM

edFile=_Peds.sum SigFile=_BeamStop.sum Vmax=0.153 Vmin=0.0





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Photographic Film

LDRD-1 Chip: ALS e- Beam Test



Test at BTS beam line of LBNL Advanced Light Source: 1.5 GeV e⁻ beam, 1 Hz rate, tunable intensity:

Pixel Size	<nb. of="" pixels=""></nb.>	<s n=""></s>
10 µm	2.71	14.8
20 µm	2.67	15.1
40 µm	2.37	15.3







LDRD-1 Chip: Irradiation Test

Radiation hardness test at BASEF Facility at LBNL 88" cyclotron: 30 MeV p beam, Flux = 7×10^7 p cm⁻² s⁻¹, Total = 1.4×10^{12} p cm²: Detector still **functional after irradiation**, observed increased leakage current, performance tested at ALS.

> Neutron irradiation at newly commissioned beam-line at energies matching anticipated ILC n background planned for end of July.

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Average Noise vs Fluence

LDRD-1 Chip: Point Resolution



Estimate point resolution using attenuated IR laser beam

- focused to $< 10 \ \mu m$ spot;
- Scan along rows and determine ηdistribution summing signal along columns;

Convert η distribution to space resolution using MC method and assuming S/N=15;

Chip	Pixel Size	Resolution
	(µm)	(µm)
LDRD-1	10	2.0
LDRD-1	20	3.3
LDRD-1	40	5.1



Method tested comparing resolution for Mimosa-5 chip from η scan to test beam data and results agree;

Time Properties of CMOS Pixel Signal



Use fast pulsed IR laser (1 ns -0.5 ms) collimated on 4x4 pixels to study signal formation and time evolution in CMOS pixel sensors:



Next Steps in CMOS Pixel R&D



Second generation chip (LDRD-2) ready for submission, in AMS 0.35 "OPTO" process. Features more complex pixel with in-pixel CDS, power cycling, different bias options and diode sizes and option of rolling

shutter for read out at high rate.

Third generation chip (LDRD-3), currently being designed, will include 4-bit fast ADCs on the chip periphery, matching 20 µm pitch and low power consumption, expect submission by Spring 07.



Concurrent work started on data sparsification (simulation, FPGA and eventually on-chip implementation) in collaboration with STAR LBNL group (Supplemental LCRD proposal).

DEPFET Irradiation Tests



Started collaboration with MPI Munich on DEPFET pixels;

First single-pixel structures being tested at LBNL: I-V curves and spectroscopic measurements;





Proton irradiation at BASEF in mid-July;

Characterisation of larger matrices in Fall and plan for collaboration on mechanical characterisation of DEPFET modules and readout;

CMOS Pixel Sensor Back-thinning



First complete characterisation of CMOS sensors before and after back-thinning using radiation with different penetration depths to study change in collected charge and S/N induced by thinning;

Thinning of diced Mi mosa-5 chips to 50 µm by wet grind and polishing;

Results from first two thinned chips (4 independent sectors) :



Back-thinning being assessed to 50 μ m, next tests to 35 μ m.

Noise	⁵⁵ Fe	Laser 850 nm	Laser 1060 nm	1.5 GeV e ⁻
(+3±7)%	(-8±8)%	(-16 ±6)%	(-16±10)%	(-5±5)%

Ladder Design, Production & Testing



LCRD and LBNL core funding support new program of design, construction and characterisation of full ladder equipped with back-thinned CMOS pixel sensors starting from STAR HFT design;

FEA started, mechanical characterisation of first prototypes in Fall, full prototype by end of 07, data will also used to study stability effects

Component	% X ₀	Si equivalent
	X	(µm)
CMOS chip	0.053	50
Adhesive	0.014	14
Kapton cable	0.090	84
Adhesive	0.014	14
CF support	0.110	103
Total	0.282	264

on physics and offline alignment.





E CONTINUE



StdHepLOIOInterface.hh

Simulation, Reconstruction and Analysis Software



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Sensor Simulation and Data Analysis in MARLIN

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Sensor simulation developed in Java/JAS for CCDs and in C++/Marl i n for DEPFET sensors, detailed simulation study of CMOS pixels needed; Implement sensor simulation (Pi xel Si m) and cluster analysis (Pi xel Ana) in Marl i n and interface to LCI 0 beam test data (Pi xel Reader) Analysis setup allows to analyze test beam data and validate simulation response on real data, estimate effect of changes in geometries and characteristics and obtain realistic digitized simulation of full physics events and overlayed backgrounds;

Use VXD01 5-layered Vertex Tracker geometry in Mokka (50 µm thick Si sensor);

Present sampling of preliminary results and plans for future simulation and validation activities at LBNL.

CMOS Pixel Data Implementation in LCI 0



VtxRawData class implemented in LCI 0:

Create VtxRawHits:

VtxRawHits* vtxData = new VtxRawHits(aDataFileName,aFrame); LCWriter* lcWrt = LCFactory::getInstance()->createLCWriter(); Create and fill header with chip geometry information: string detName("MIMOSA V - det02"); runHdr->setDetectorName(detName); runHdr->parameters().setValue("NRows" , vtxData->getNRows());

Store ADC, Noise and Pedestal (if update online), otherwise, just store ADC and read initialisation Noise and Pedestal from Condition Database;

TrackerRawDataImpl* vtxRaw = new TrackerRawDataImpl ;
vtxRaw->setCellID0(vtxData->getIndex(iRow,iCol,aFrame)) ;
vtxRaw->adcValues().resize(3);

vtxRaw->adcValues()[0]=10*vtxData->getADC(iRow,iCol,aFrame);

Sensor Simulation



Standalone Geant 4 beam test simulation for ALS and BASEF PAHEREwtParticle bh" setup;

Develop sensor simulation starting from VTXDi gi Processor written by A. Raspereza as Marl in package;

Use SimTrackerHit points of impacts from Mokka model energy loss fluctuations with G4; Define pixel geometry and epi-layer thickness according to chip to be simulated, treat diffusion coefficient as free parameter, accounting for inter-pixel coupling, and adjust to fit cluster size, interface to Pi xel Ana provides TrackerPul se and TrackerRawData data;



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Pi xel Ana starts with TrackeRawData (**pulse height** and initial noise and pedestal), flags **noisy** pixels, updates noise and pedestal values, performs **cluster** search and generate TrackerHi t data:



<u>1st Algorithm</u>: set two S/N thresholds for seed and additional pixels to be added to cluster;

<u>2nd Algorithm</u>: set S/N threshold for seed pixel and add fixed matrix of neighbor pixels.

Characterize cluster shape in terms of pixel multiplicity projected over major and minor cluster axis.

Pixel Configurations and Data Sets



Several test beam data sets converted into LCI 0 format and used for validation of pixel simulation:



Cluster Pulse Height, Cluster Size



Cluster reconstruction: 1st Algorithm



Cluster Pulse Height, Cluster Size

Cluster reconstruction: 2nd Algorithm

Fraction of Total Charge in Cluster vs. Nb. of Pixels

Cluster Pulse Height peak vs. Matrix Size







Single Point Resolution



Determine single point resolution for single tracks using charge center of gravity with no magnetic field;

Compare single point resolution from simulation to data using beam for Mi mosa 5 and focused Laser scan for LDRD-1:

2500	1.	. [20 µm
1500			
1000	н		
-8.05 -0.04 -0	0.03 -0.02 -0.01 0	0.01 0.02	0.03_0.04_0.05
		ZRO	eco - ZGen (mm)
	12.14	ZRO	eco - ZGen (mm)
Chip	Pixel Size	Data	Simulation
Chip	Pixel Size (µm)	Data (µm)	Simulation (µm)
Chip LDRD-1	Pixel Size (µm) 10	Data (μm) 2.0	Simulation (µm) 1.5
Chip LDRD-1 LDRD-1	Pixel Size (μm) 10 -20	Data (µm) 2.0 3.3	Simulation (µm) 1.5 3.2
Chip LDRD-1 LDRD-1 LDRD-1	Pixel Size (μm) 10 20 40	Data (µm) 2.0 3.3 5.1	Simulation (μm) 1.5 3.2 5.5

Single Point Resolution



Single Point resolution vs. track polar incidence angle for Mi mosa 5 shows only minor effect in z: Hit Resolution (µm) 17 µm 1.8 1.6 1.4 R-Phi 1.2 z 0.8 0.6 20 25 30 35 40 Angle w.r.t. Normal Incidence Hit Resolution (µm) 3.5 3 2.5 2 1.5 15 20 25 30 35 40 45 S/N

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Single Point resolution vs. Signal-to-Noise ratio for LDRD-Chi p 1 20 µm pixels:

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Pixel Response to Inclined Tracks

Study response to inclined tracks in terms of <u>cluster size</u> and <u>cluster shape</u> for different pixel sizes;

Started validation of simulation results with beam test data for LDRD and Mimosa 5 chip on 1.5 GeV e⁻ beam at ALS;

Signal scaling as $\sim \cos \theta$



verified on Mimosa5 on 120 GeV π beam test data by Strasbourg group;

Cluster size change controlled by ratio of epi-layer thickness and pixel size and is modest for typical values.

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Pair Background





Study pairs generated with Gui neaPig program for TESLA 500 GeV parameters and tracked through VXD01 using Mokka

Pair Background



Cluster Size



Significant difference in cluster size and cluster shape for low momentum e- from pairs, compared to high energy e⁻ may be useful for identifying and rejecting background hits in pattern recognition; Beam test using tunable energy e⁻ beam (50 MeV-0.5 GeV) from LOASIS plasma accelerator facility at LBNL planned for Fall 06 to validate simulation results.

Pixel Telescope for LBNL 1.5 GeV e⁻ beam



Developing small Pixel telescope prototype for use at ALS e⁻ beam;

2 & 3 planes of 50 μ m back-thinned Mi mosa-5 sensors (17 μ m pitch) providing < 5 μ m resolution on DUT



Telescope will enable studies of tracking efficiency on LBNL beam and systematic investigations of pixel response vs. point of impact.



Pixel Telescope for Fermilab

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Developed LCRD proposal to duplicate EUDET telescope Demonstrator based on 6+1 planes of Mimostar-3 CMOS pixel sensors, providing 1 µm extrapolation resolution on DUT;

Collaboration with IHPC, Strasbourg would provide sensors and DAQ at production cost, testing and assembly to be performed at LBNL;

Online and offline software can be shared with EUDET, providing US groups with performant telescope at minimal cost and comparable setup to EU groups making performance comparisons and data exchange easier and reliable.



Two new CMOS chips in the LDRD series expected to provide building blocks for pixel chip meeting the ILC specifications by end 07:

- < 3 μ m single point resolution,
- fast readout (~25 μ s / column),
- low power consumption (<100 μ W / channel),
- on pixel CDS,
- in-chip 4-bit ADC

New activities addressing data sparsification, integration issues and beam test facility at the center of new LCRD proposals;

LCRD funding promoting new project to design, construct and characterise functioning ladder equipped with back-thinned chips meeting the ILC material budget specs.



Sensor simulation and validation within Mokka+Marlin framework started at LBNL

Systematic program of simulation validation:

- Low energy e⁻ at LBNL accelerators;
- High energy π require plans of beam tests at CERN and/or FNAL;

Soon extend studies from single tracks/VTX only to benchmark processes with patrec, backgrounds and full LDC (and possibly SiD) tracking;

Setting up VTX and physics simulation group at LBNL, aim at collaborating with other interested groups and develop significant visitor program to foster cooperation and acquire needed know-how in modeling, simulation and reconstruction.



White Paper on ILC Vertex Tracker R&D as first assessment of R&D directions, priorities and activities produced by the community under a common authorship first proposed at Snowmass 2005;

Further discussion at ECFA ILC workshop in Vienna and plan agreed at recent Ringberg ILC VTX workshop;

- for internal use in the ILC VTX community to assess R&D time and define common specs and references for guiding R&D prog
- as backbone document to support projects w/ funding agencies a
 as reference for new groups joining;

Address inter-dependences with detector concepts but not concept-specific.



<u>Proposed editors</u> : L. Andricek, M. Battaglia, B. Cooper, T. Greenshaw, M. Caccia

<u>Action lines</u> :

- Sensor technologies
- Simulation and Software tools
- Mechanics and Integration
- Optimisation
- Decision making process, Costing
- Inventory of facilities

Significant to have draft by end of the year, then evolve with Annual Reports and back-up documents.