SMTF R&D Status

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SMTF Institutions & Contact Persons:

Argonne National Laboratory: *Kwang-Je Kim*
Brookhaven National Laboratory: *Ilan Ben-Zvi*
Center of Advanced Technology, India: *Vinod Sahni*
Cornell University: *Hasan Padamsee*
DESY/TESLA: *Dieter Trines*
Fermi National Accelerator Laboratory: *Robert Kephart*
Illinois Institute of Technology: *Christopher White*
INFN*: *Sergio Bertolucci, Giorgio Bellettini and Carlo Pagani*
KEK: *Nobu Toge*
Lawrence Berkeley National Laboratory: *John Byrd*
Los Alamos National Laboratory: *Patrick Kelley*
Massachusetts Institute of Technology: *Townsend Zwart*
Michigan State University: *Richard York*
Northern Illinois University: *Court Bohn*
Northwestern University: *David N. Seidman*
Oak Ridge National Laboratory: *Stuart Henderson*
Stanford Linear Accelerator Center: *Chris Adolphsen*
Thomas Jefferson National Accelerator Facility: *Swapan Chattopadhyay*
University of Pennsylvania: *Nigel Lockyer*
University of Rochester: *Adrian Melissinos*
University of Wisconsin: *David Larbalestier*
*: INFN is discussing its possible contribution to SMTF.

SMTF ILC Goals

Establish a high gradient, 1.3 GHz cryomodule test area at Fermilab with a high quality pulsed electron beam using an upgraded A0 photo-injector.

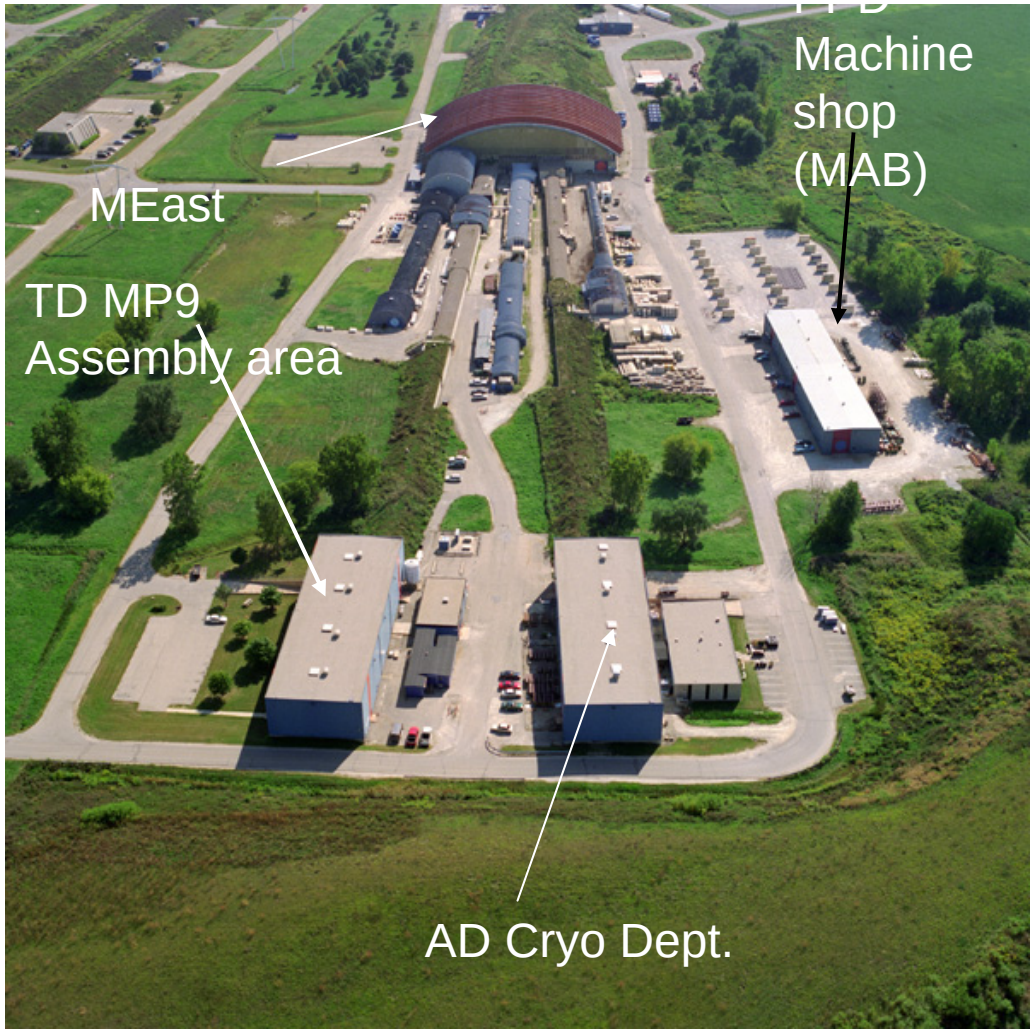
Establish a factory with infrastructure for the assembly of prototype cryomodules using cavities produced at collaborating institutions and industries.

Fabricate and Test 1.3 GHz high gradient prototype cryomodules in collaboration with laboratories, universities and US industrial partners.

Demonstrate 1.3 GHz cavity operation at 35 MV/m with beam currents up to 10 mA at a ½ % duty factor.

Develop the capability to reliably fabricate high gradient and high-Q SRF cavities in U.S. industry.

Meson Building at Fermilab



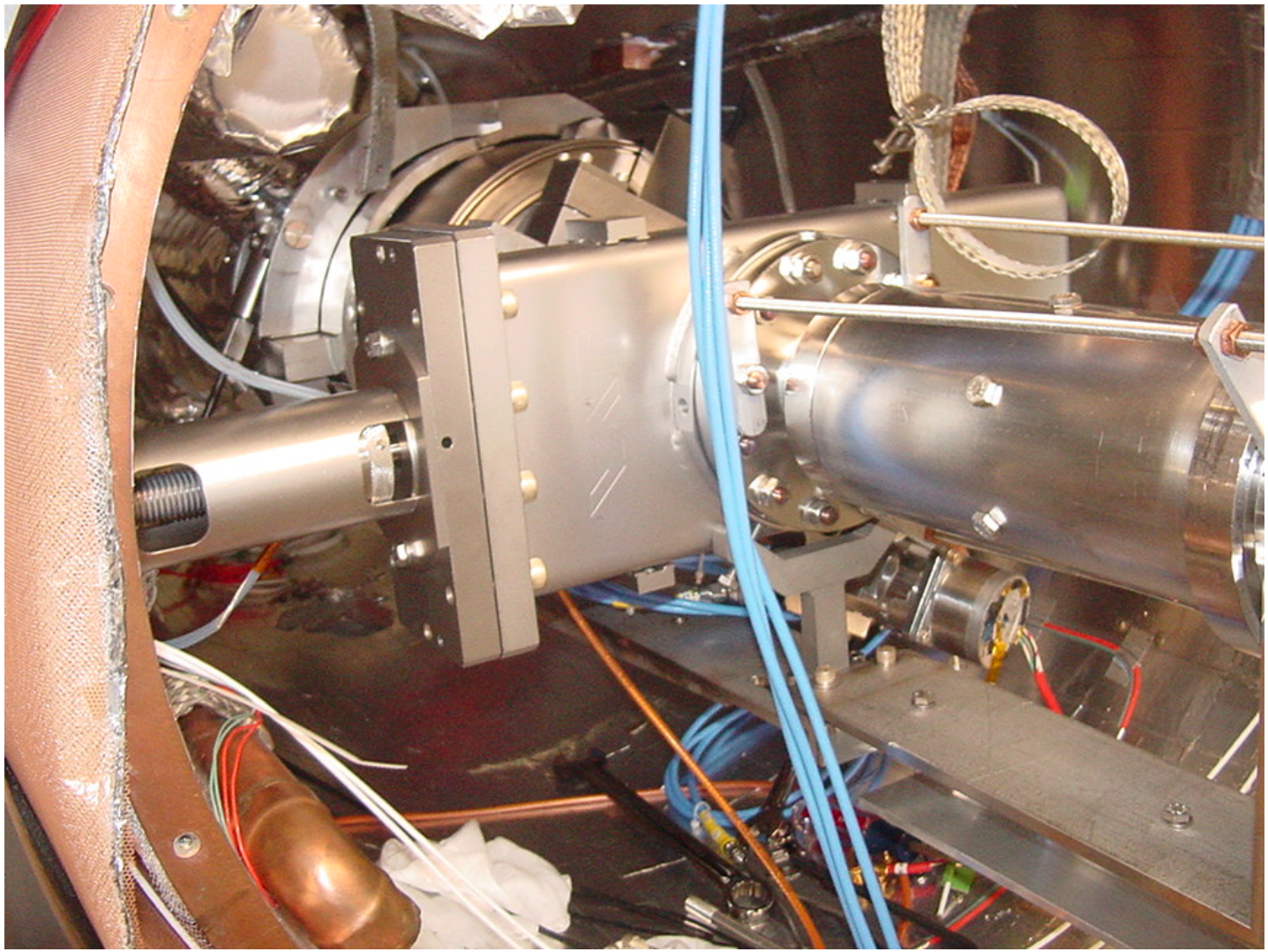
Meson Starting as a Bone yard

Meson Now

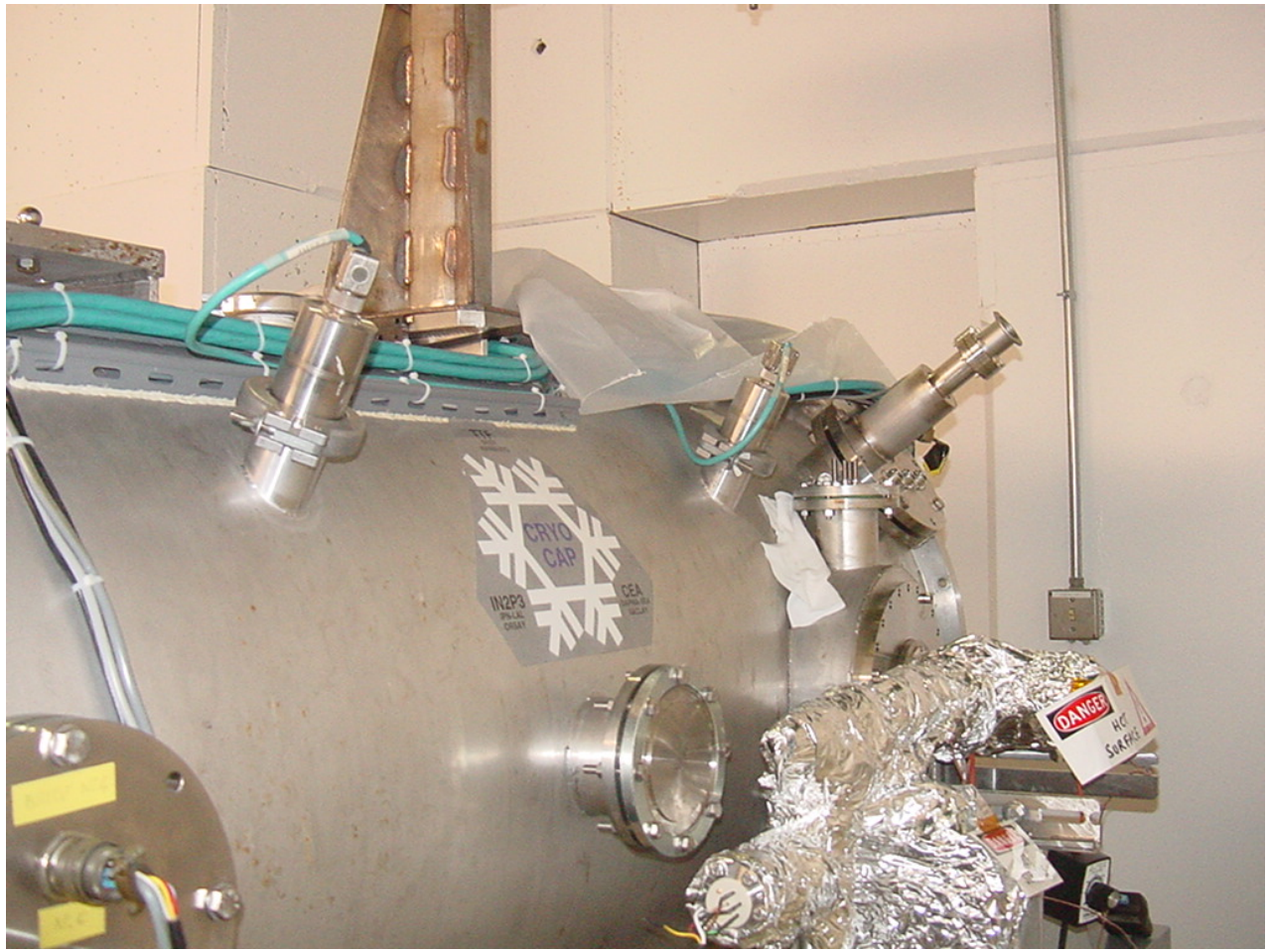
Capture Cavity II (cave)

Destination is A0 Injector H. Edwards et al.

Capture Cavity II



Input Coupler CCII



Processing of SMTF Input Couplers FNAL & SLAC

Cryogenics Flowing

Helium storage for Capture Cavity II

RF Hut & Power proceeding

CCII left out of picture & “Chechia” Cave to right

Klystron and Waveguide

Circulator

New Muon Lab (ILCTA)

Chicago Cyclotron Magnet being dismantled

Cryomodule Beamline

Location planned for 4 cryomodules & A0 injector

SMTF R&D Goals 06

- Cavity Fabrication
  - Fermilab is fabricating cavities with industries (12 Cavities)
  - 8 Dressed Cavities from DESY (exchange for 3.9 GHz Cavities)

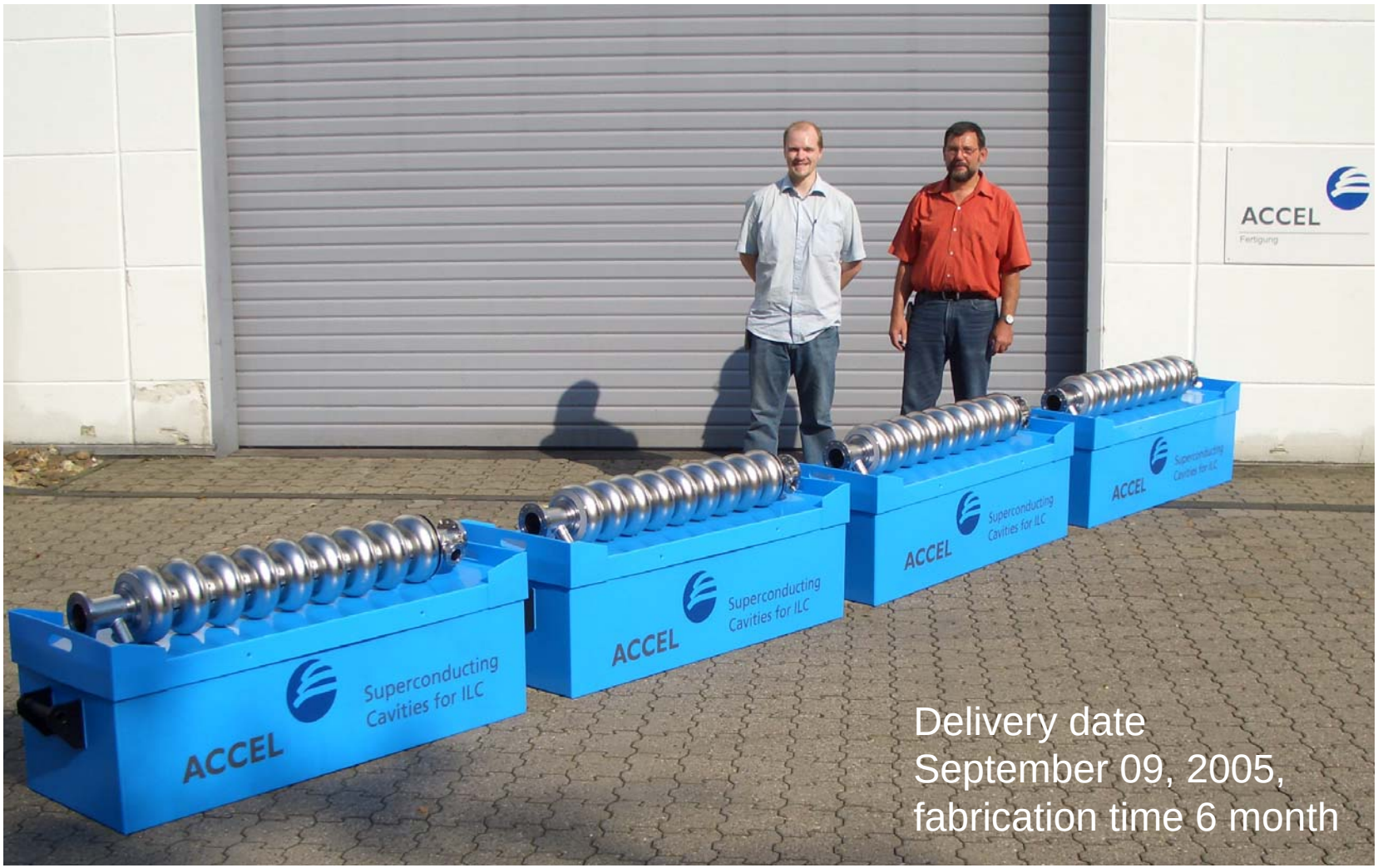
- Cavity Processing & Testing Infrastructure & Technology Development
  - Upgrade of the Cornell (BCP) and Jlab (EP) Facility
  - Development of the BCP parameter at Cornell (25 MV/m)
  - Development of the EP parameters at Jlab (35 MV/m)
  - 25 MV/m cavities fabricated and Tested (VDT/HDT @ Fermilab) with BCP using US industrial production and FNAL/ANL processing.
  - Study and Develop infrastructure for EP at FNAL/ANL

- First US assembled cryomodule Type III+ to study design, participation in fabrication and cost reduction.
- International collaboration on the Design of an ILC Cryomodule
- Develop industrial base in US for Main Linac Components

Cavity Plan

- Received 4 TESLA design 1.3 GHz cavities from ACCEL.
  - BCP and Vertical test at Cornell. AES and Fermilab staff will participate in the work. Goal is to develop 25 MV/m BCP parameters.
- Jlab will electro-polish, vertical test and dress. Proposed to Jlab that FNAL staff & SMTF collaborators will participate in these activities. The goal is to develop 35 MV/m EP parameters.
- Horizontal testing and string assembly will take place at Fermilab. Fermilab is developing infrastructure.
- Ordered 4 (8) cavities from AES. These cavities will follow the same path as ACCEL cavities.
  - At present we are going through all the DESY drawings for 1.3 GHz cavity
  - Purchased Nb for 12 cavities and scanning at Fermilab
  - Expect cavities by early summer 06.

ACCEL Cavities @ FNAL



ILC Cavities Plan

- Four cavities from DESY to get the tooling and processing infrastructure started at Cornell and Jlab ASAP.
- One cavity from DESY (Capture Cavity) to get the Meson infrastructure up and running.
- US-Japan agreement to provide 4 processed and VDT tested cavities.
- 8 Dressed cavities from DESY. These cavities will be electro polished, vertical test, Dressed and horizontally tested and sealed. (This is in exchange of 3.9 GHz cavities and cryomodule Fermilab is fabricating for DESY.)
- Develop Reentrant cavity and Single crystal (Standard Design) cavities.

ILC Cavity Processing

- 4 DESY cavities will be used to develop tooling, initial processing etc. at Cornell, Jlab and ANL for the processing of 1.3 GHz cavities.
- In the Phase I the plan is
  - Upgrade infrastructures at Cornell (BCP) and Jlab (EP) to process and vertical test 1.3 GHz cavities.
  - Use the Cornell BCP and VDT facility to develop BCP parameters (25 MV/m).
  - Use the Jlab EP and VDT facility to develop EP parameters (35 MV/m).
  - Develop HPR, BCP and EP facility at FNAL/ANL

Cavity Processing

- In Phase 2 (Tight Loop Production and Processing)
  - Use cavities produced by industry
  - Process cavity at FNAL/ANL BCP
  - Study development of an EP facility at FNAL/ANL
    - Discussion has taken place between Fermilab, LANL, ANL,JLAB, DESY, and KEK to develop a EP facility for ILC.

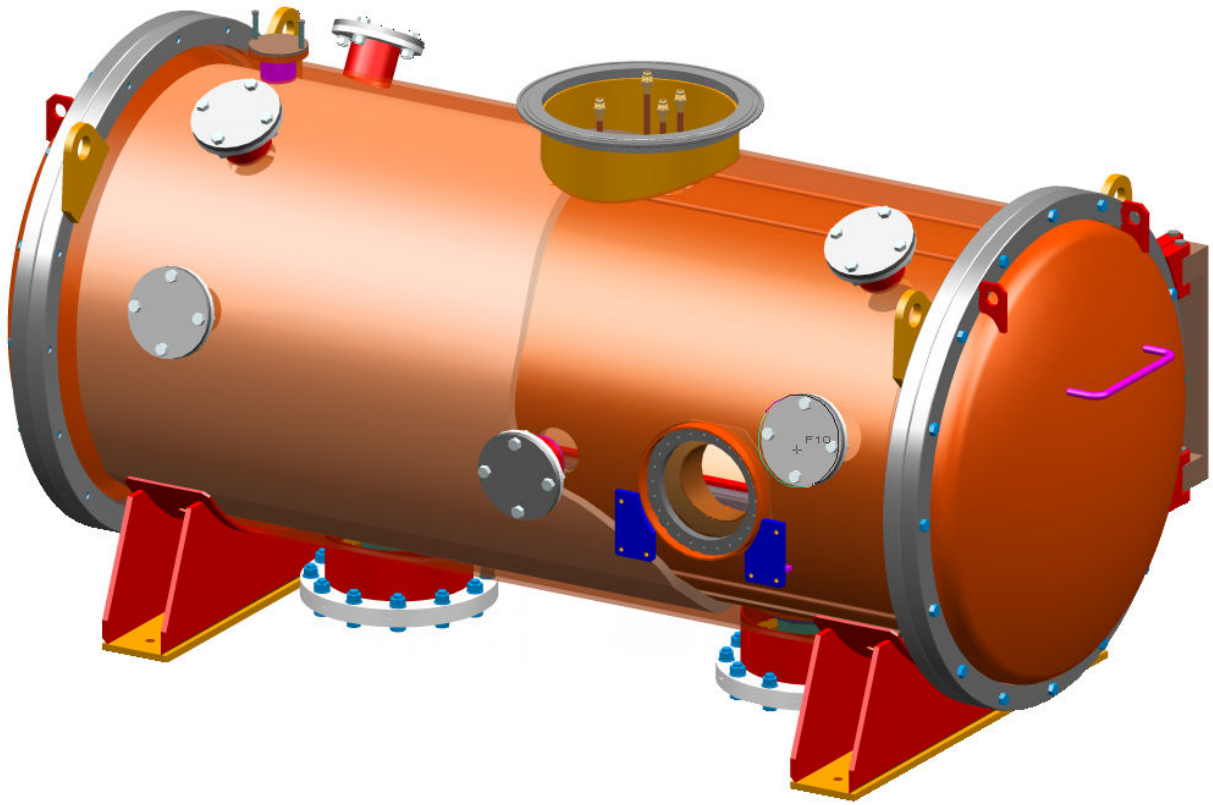
At the end of this phase we will have two facilities each in US for BCP and EP Processing capable of producing 35 MV/m cavities.

1) BCP facilities at Cornell and ANL/FNAL
2) EP facilities at Jlab and ANL/FNAL

Infrastructure for ILC Cavities

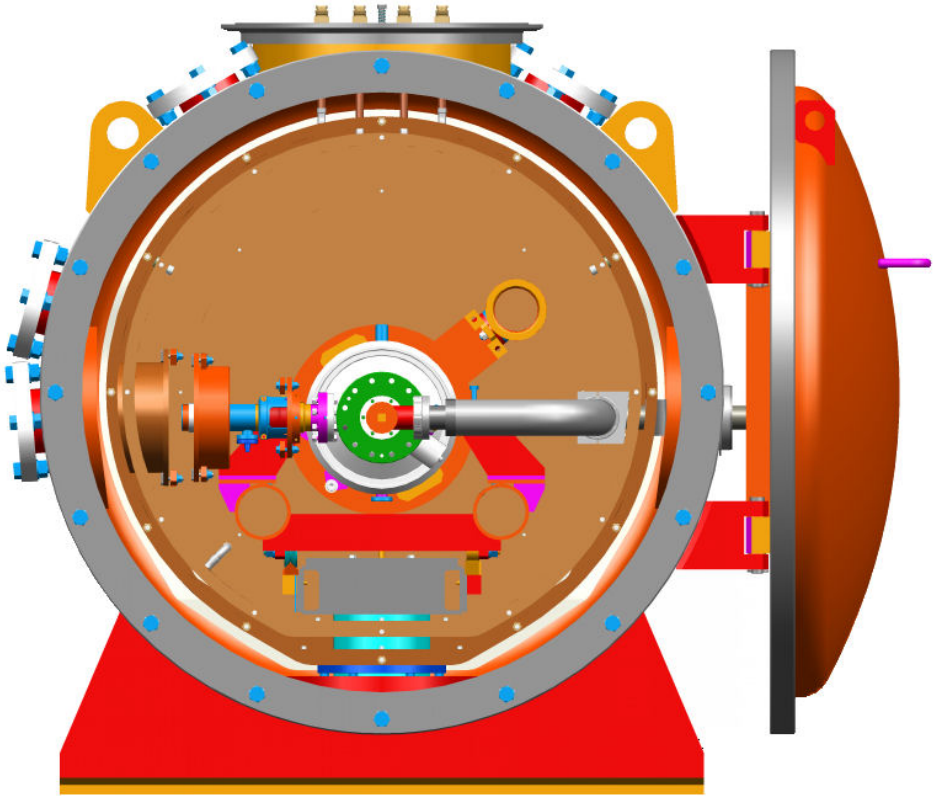
- Infrastructure at Cornell and Jlab needs upgrade to process the 1.3 GHz cavities.
- Fermilab is working on installation and commissioning of the BCP facility at ANL (FY06)
- Fermilab has design and placed an order for clean rooms and assembly fixture for these cavities and its dressing for the Horizontal test. This is part of the Cryomodule Assembly Facility.
- Fermilab is building a horizontal test stand and plans to build a vertical test stand. Need cryogenic, RF Power, controls etc. (on schedule to begin commissioning May06
- We need to develop a design for an EP facility at ANL/FNAL.

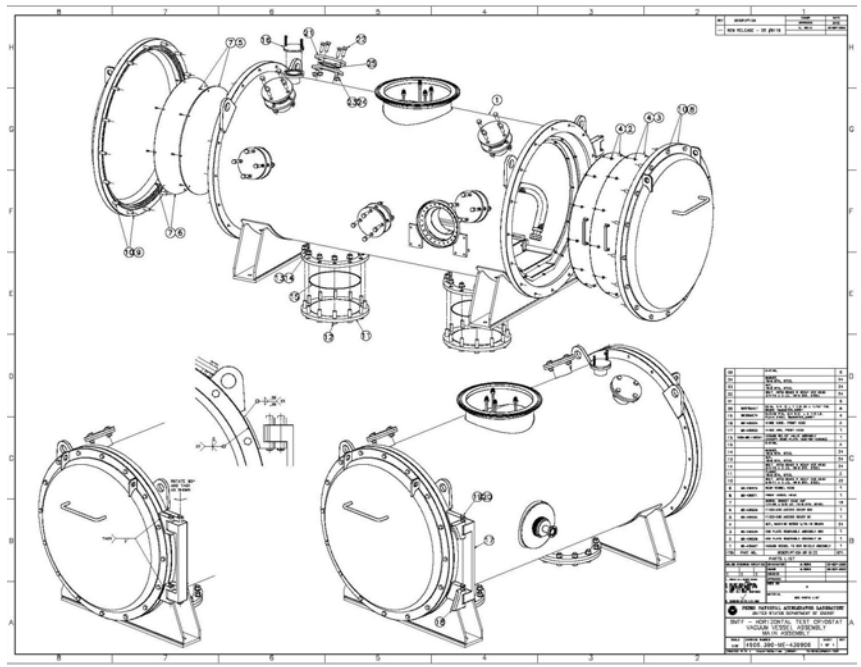
Horizontal Test Facility “Chechia”



SMTF Horizontal Cryostat – vacuum shell is hidden to reveal superinsulation and 80K thermal shield

“Chechia” End View





Helium Vessel with a 1.3 GHz RF Cavity Within the Horizontal Cryostat

Joint ANL/FNAL Processing Facility

Chemical Processing Rooms

Air Scrubber

Cryomodule Design and Fabrication

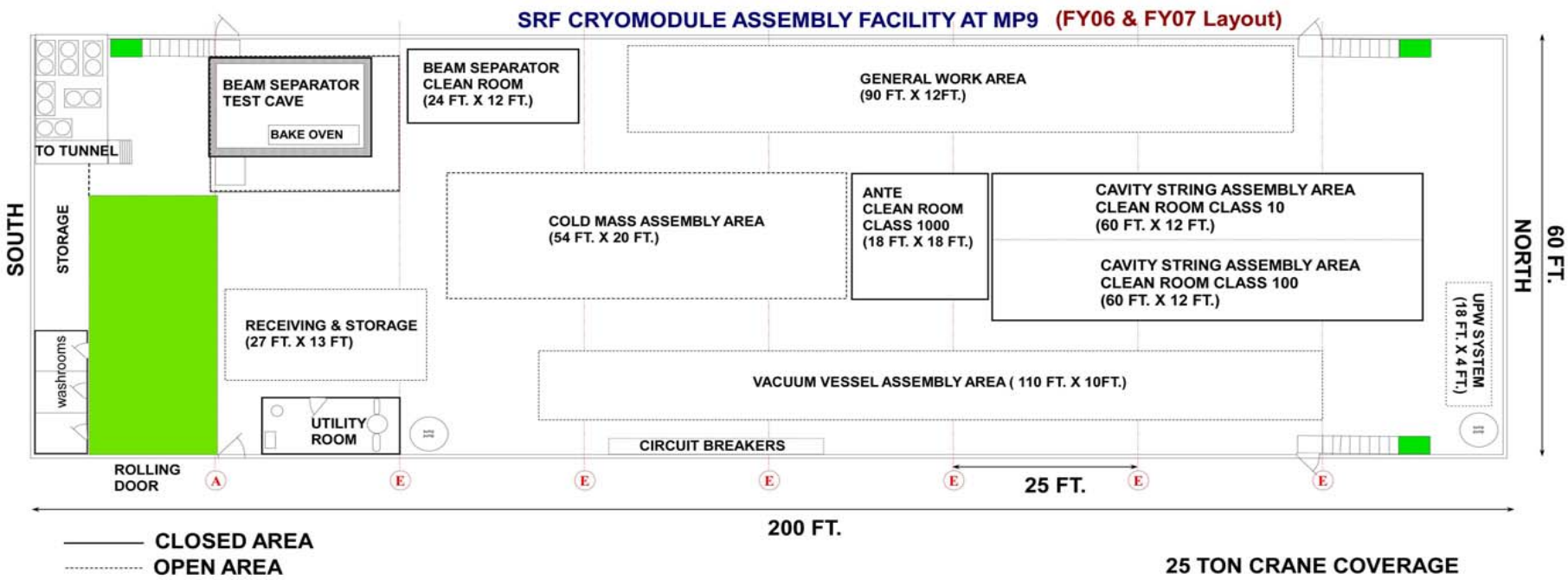
- In FY05 we started converting the DESY & INFN design of the ILC cryomodule in the US system.
- This work is almost complete and we are in position to order parts for a cryomodule fabrication using the 20 cavities we expect to have by mid FY06.
- The cryomodule is the significant cost in the Main Linac. Industrial fabrication and cost reduction are important issues that we need to start now.
- Fermilab with its considerable experience in assembling large object can help improve the design and fabrication of ILC cryomodule design.

Cryomodule Design

- Fermilab has started a global discussion on the ILC Cryomodule design. (DESY, INFN, KEK and Fermilab)
- The current design does not have all the knowledge from the cryomodule fabrication at DESY.
- Also there exists a general view is that current design needs to evolve. (The goal of WG2 is to address this issue)
- Fermilab has been in discussion with two companies who plan to participate in cryomodule fabrication with a view of fabricating it at their factory at a later date.
- Fermilab plans to work towards the ILC cryomodule design after it has experience in building TTFIII+

Cryomodule Assembly Facility (MP9)

- Cavity will be dressed in CAF for horizontal test at meson building
- Horizontally tested cavities will be assembled into a string at CAF.
- Cryomodule fabrication takes place at CAF.
- Single cryomodule will be tested at either new muon or meson



Ordered and complete by March06

String Assembly at CAF

The assembly of a string of 8 cavities into a string. Class 100 clean room at DESY

Similar facilities being constructed at Fermilab in the Technical Division (MP 9)

The inter-cavity connection is done in class 10 cleanroom

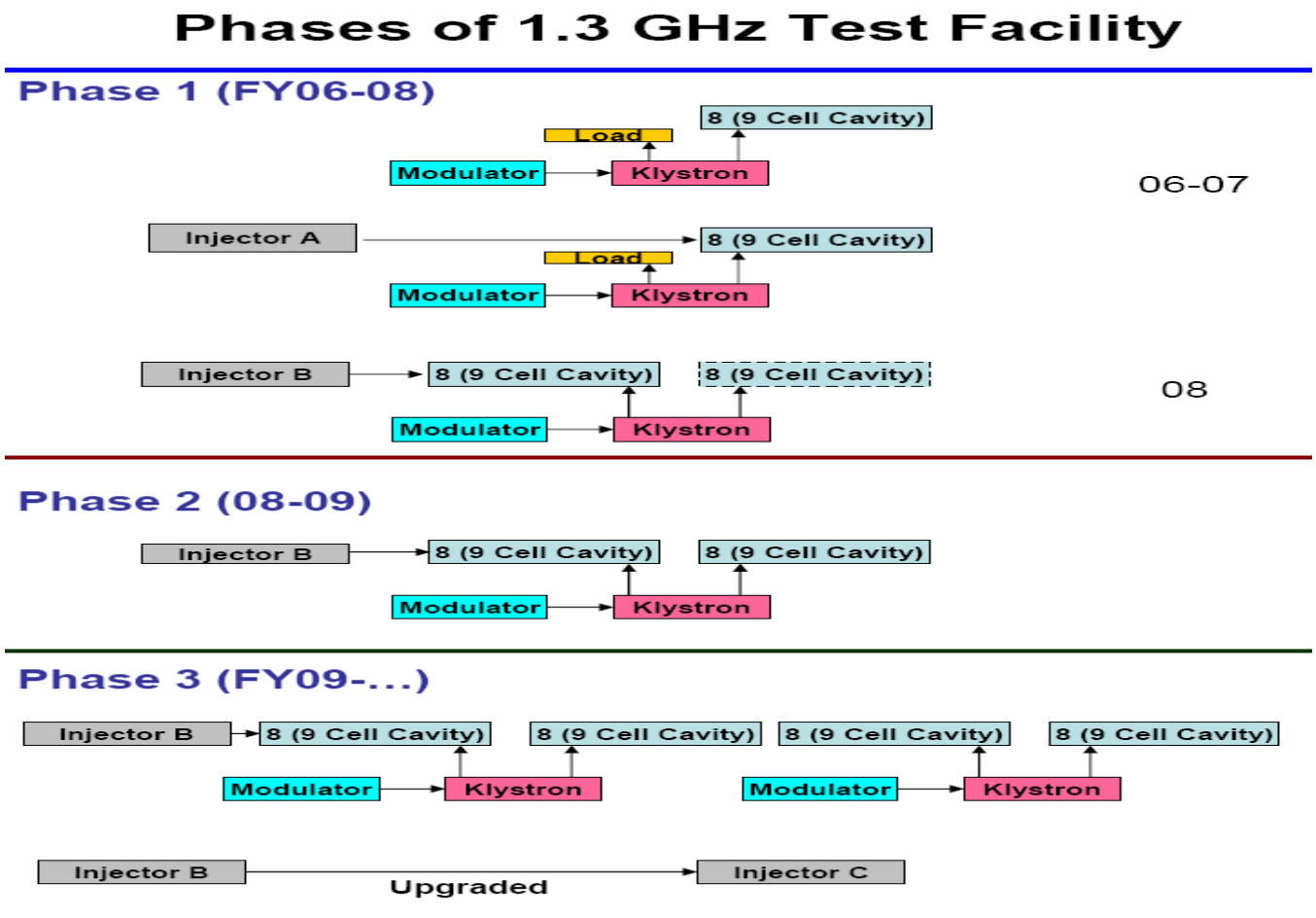
Module Assembly at CAF

Cryomodule assembly facility is also being built in the Technical Division's (MP9) building

Similar in size and tooling to the DESY facility

Larger facility later in ICB

Cryomodule Plan



Year	Cryomodule Number
06	1
07	2
08	3
09	4-5
10	5-6

By FY09, four ILC cryomodules & beam

Deliverable: Fully tested basic building blocks of the Main ILC Linac.

Penn LLRF Plans

- Developed cavity simulator (quite advanced)

http://rutherford.hep.upenn.edu/~lockyer/llrf.html

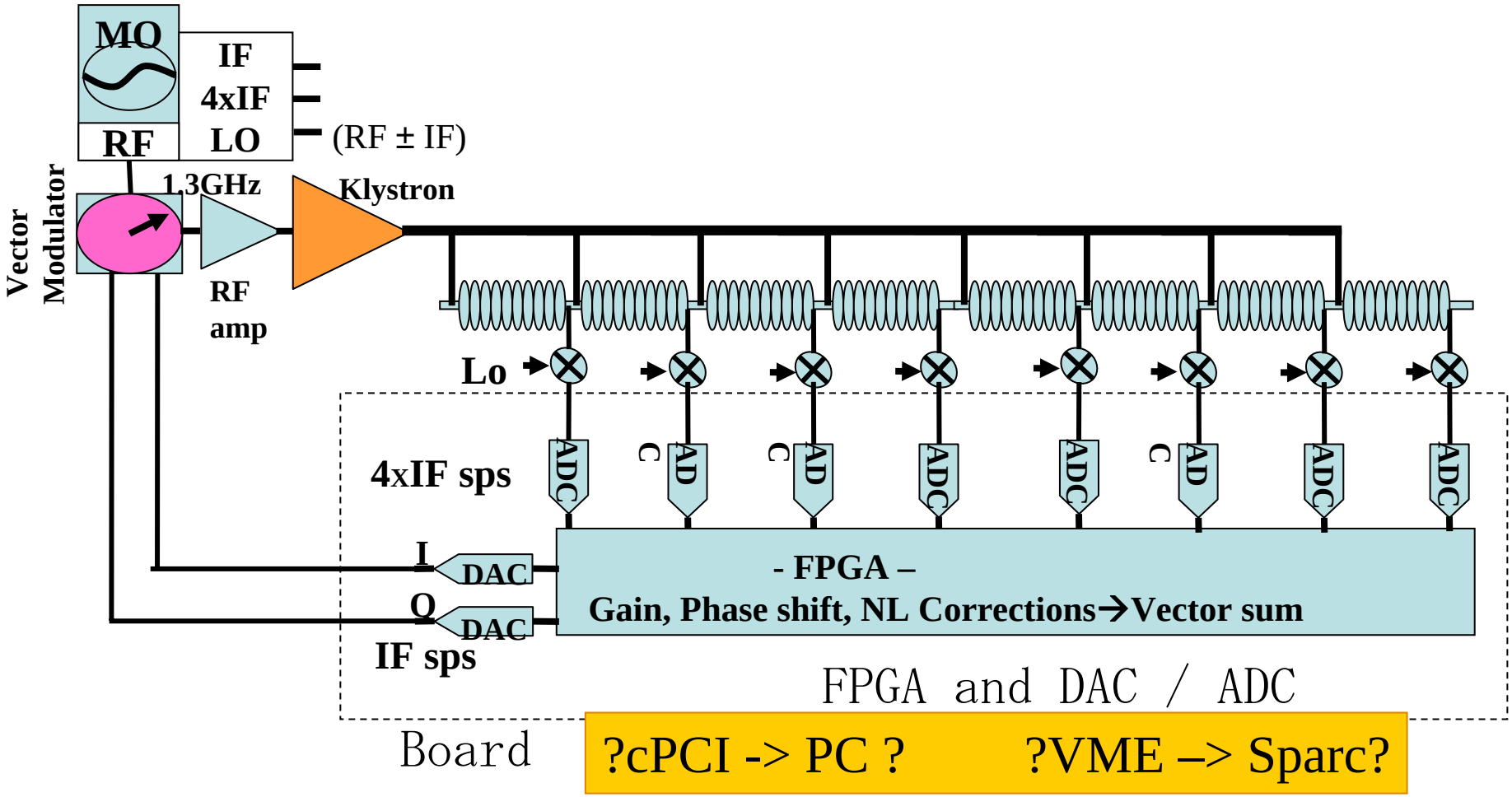
- Follow Simrock architecture
- Implement using commercial products to establish baseline
- Platform to develop software
- “Lyrtech” board compatible with DESY “Simcon 3.1”
- Merge with capture cavity LLRF at Fermilab for testing
- Exercise and calibrate simulator based on FNAL “Chechia”
- Implement LLRF on SMTF modules
- Develop LLRF control HW design document

Cavity Simulation Effort

- Single Cavity simulation implemented (T. Schilcher thesis)
  - Lorentz force effects included
  - Phase jitter
  - Feed Back implemented with drive limits.
  - Beam
- Near Future
  - Feed Forward
  - Multiple cavities –

Work done by Penn 1st year graduate student Justin Keung

Basic Digital LLRF Components



ADC / DAC Board

HIGHLIGHTS

- Eight 105 MSPS Input channels
- Optional Add-On daughter board provides 8 additional input ADC channels or 8 output DAC channels and a Virtex-II FPGA processing board.
- Compact PCI (32-bit cPCI, 33 MHz) 6U form factor
- FPDP interface with 400 MB/sec transfer rate (gives 12.5 MSPS per channel at 8 channels and 25 MSPS at 16 channels)
- Low level hardware drivers API and GUI
- High level hardware drivers integration in Simulink Blocksets for quick implementation with System Generator for DSP
- Leading edge communication interface allowing data recording and playback on the on-board SDRAM

KEY FEATURES & BENEFITS

- Software-Selectable programmable gain amplifier on each channel
- External Clock & External Trigger Inputs (Multiple in-phase board can be used with the external clock)
- Programmable Sampling Clock (1-105 MHz)
- 34-pin External Virtex-II GPIO Header
- Low- and High-Level drivers well tailored to each development approach.
- High-Level Simulink Blocksets include control tools for the GPIOs, Trigger, programmable gain, SDRAM, and sampling clock.
- Communication interface to control VHS-ADC parameters modification without interrupting the DSP application when used with SignalMaster.
- Help files, tutorials, demos and documentation for quick start.

Technical Specs

Analog to Digital Converter
- 8 or 16 Analog Devices' AD6645
- Single channel 14-bit ADC
- Up to 105 MSPS guaranteed
- 100 dB Multitone SFDR 75 dB SNR (fin=15MB)
- DC to 270 MHz Analog Input Bandwidth

Analog Input Programmable Gain
- 8 or 16 Programmable Gain Amplifiers CLC5523 (Hardware Option)
- 30 MHz Bandwidth, 26 dB Dynamic Range
- 100 MHz Bandwidth, 17.5 dB Dynamic Range
- 200 MHz Bandwidth, 14 dB Dynamic Range

Analog Input
- 50-Ohm MMCX Connectors
- +/- 1.12 Vpk Full Scale Input With Programmable Gain Bypassed

Optional Low Pass Input Filter
- Optional external LPF filter or BP can be supplied for specific applications

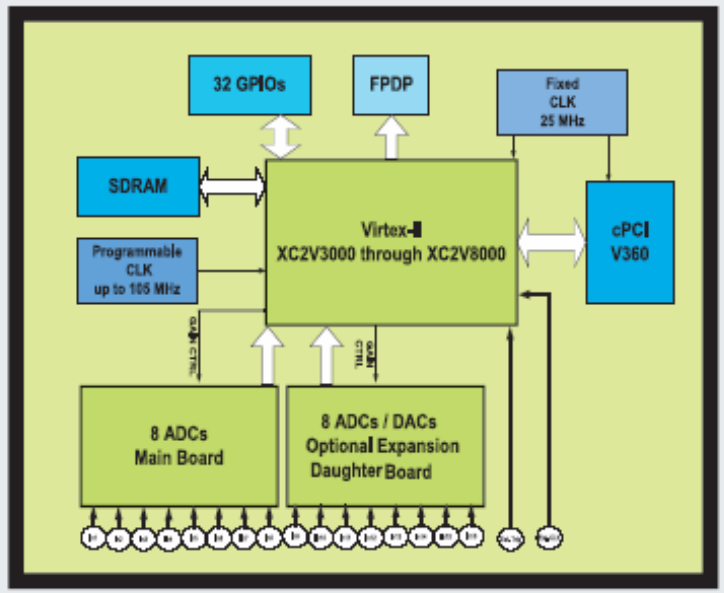
Sampling Clock
- Software-selectable on-board or external clock
- On-board programmable clock source FS6377 up to 105 MHz with 10 KHz precision
- External clock source (TCL/LVTTL/LMOS/LVCMOS) 50 Ohms

Control & Pre-Processing Virtex-II
- Pre-Processing Virtex-II FPGA (signal decimation or filtering)
- Up to XC2V8000
- SDRAM option: 2 x 16 MB or 2 x 32 MB or 2 x 64 MB

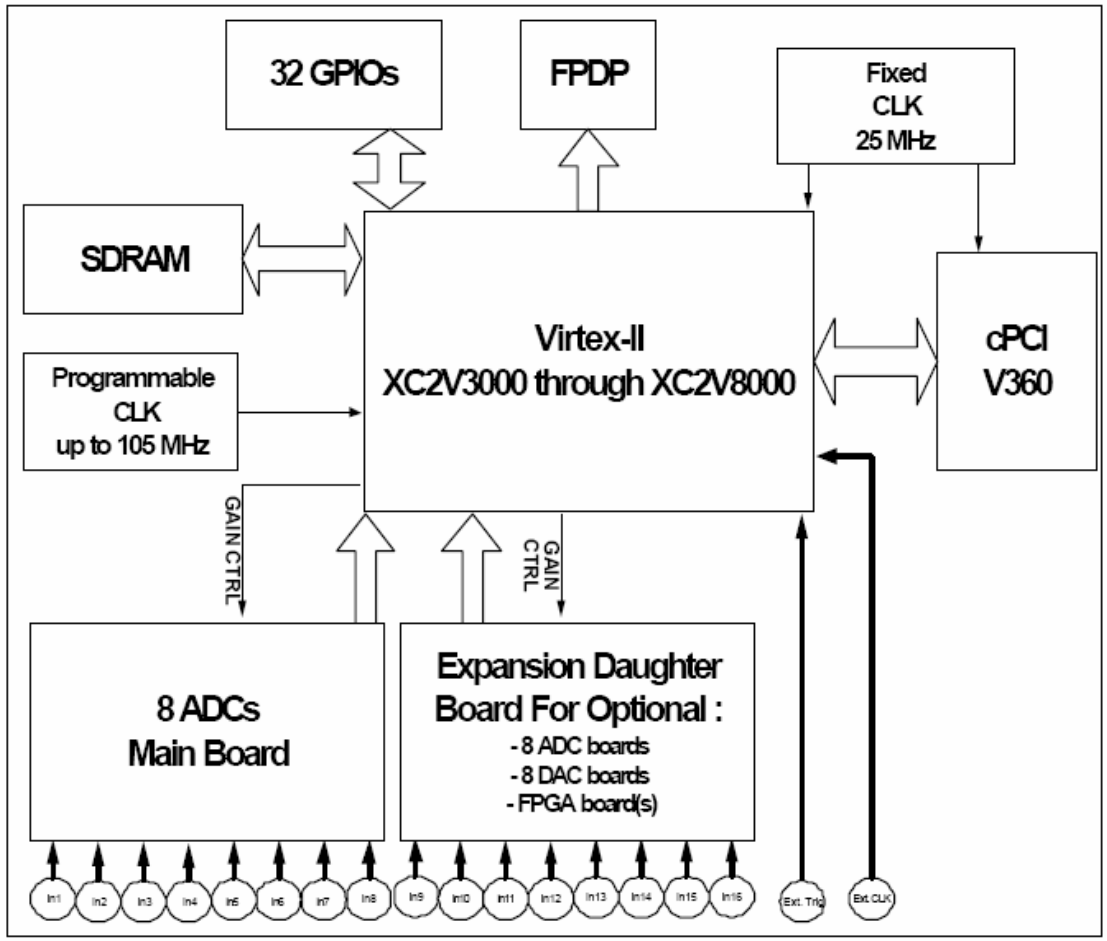
Off-Board Communication Channels
- FPDP External Port with 400 MB/sec. TDM raw data for all 8 or 16 Input Channels
- 32-bit PCI External Port, 33 MHz Control Interface
- 34-pin External Virtex-II GPIO Header with 6 optional Virtex-II LVDS giving 5Gb/s

Development Tools
- C-Coded low-level drivers and VHDL library
- MATLAB®/Simulink Blockset
- Xilinx Foundation ISE
- Xilinx System Generator for DSP

BLOCK DIAGRAM



VHS-ADC Board Architecture



Simcon 3.1 Board Comparison

Function	Simcon 3.1	LyrTech VHS-ADC
Bus Standard	VME 10MHz 32bit	cPCI 33MHz 32Bit
A/D	AD6645 10ch	AD6645 8 (16max) ch
Buffer Amp	AD8139 (2.5nV)	AD8138 (5nV)
D/A	AD9772A 4 ch (14bit)	AD9767 8 ch (14bit)
FPGA	Virtex II 4000	Virtex II 6000
Optical I/O	2 @ 3.6 Gb	- - - -
Digital I/O	2 bits	6 Differential 24 SE (5GHz)
Direct FPGA Data bus	- - - -	Front Panel Data Port 32Bit 100MHz
S/W compiler	Leonardo Spectrum ($30k ??)	MatLab / Simulink C, Xilinx development
Cost	Not Available Yet ??	16K (with FPGA SW) now

Simple SMTF Master Oscillator

- 81.25 MHz Base (A0 laser)
- 1.3 GHz generated as 16 x 81.25

  81.25 MHz @ 160dB

  1.3GHz @ (-165 +24)db = 141db Sprinter

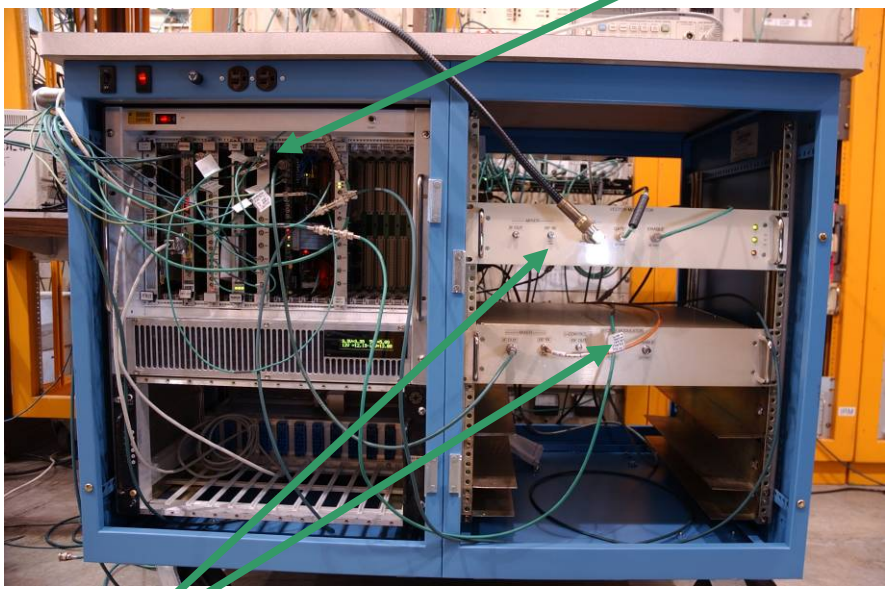
  @ (-176 +24)db = 152db ULN
- IF 81.25 MHz or 4/5 (81.25MHz) undersample ?
- Additional clocks?

Cost for Wenzel Sprinter version ~ 6K

Wenzel ULN version ~ 10K

CC2 Stand-alone LLRF System

The CC2 LLRF Portable Rack was commissioned at A0 and is ready to support CC2 operations



Drive Vector Modulator and Downconverter
Vector Modulator/Mixer (New FNAL design, upgradeable to 3.9 GHz operation)

VME Modules:

-Sparc CPU-56 running DOOCS and Matlab

-8-Ch Timer Module (FNAL design)

-8-Ch, 10 MHz fast digitizer (DESY design)

-8-Ch Function Generator board (DESY design)

-Simcon 2.1 FPGA board (DESY design +

Summary

- Considerable progress in FY05 towards SMTF proposal plan at Fermilab

- Plan for ILC SRF R&D in FY06 that includes expertise from around the world.
  - Cavity Processing and Testing
  - Cryomodule Design and Construction
  - Development of test infrastructure
- RF Power work proceeding FNAL & SLAC
- LLRF work proceeding for test facility
  - Building collaboration to develop system
  - Capture cavity two work well on its way

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- Thanks to Fermilab colleagues:
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- Thanks to Penn colleagues
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