Monolithic Pixel Detector R&D for the ILC Vertex Tracker at Berkeley

Marco Battaglia
UC Berkeley and LBNL

Si Sensors for the ILC Vertex Tracker

Vertex Tracker has to provide flavour tagging capabilities extending from high efficiency b- and τ- identification at high energies to b/c discrimination with low contamination;

Sensors with O(1μm) single point resolution and minimum thickness O(50μm);

Electronics with fast readout, on-chip zero suppression and neutron tolerant;

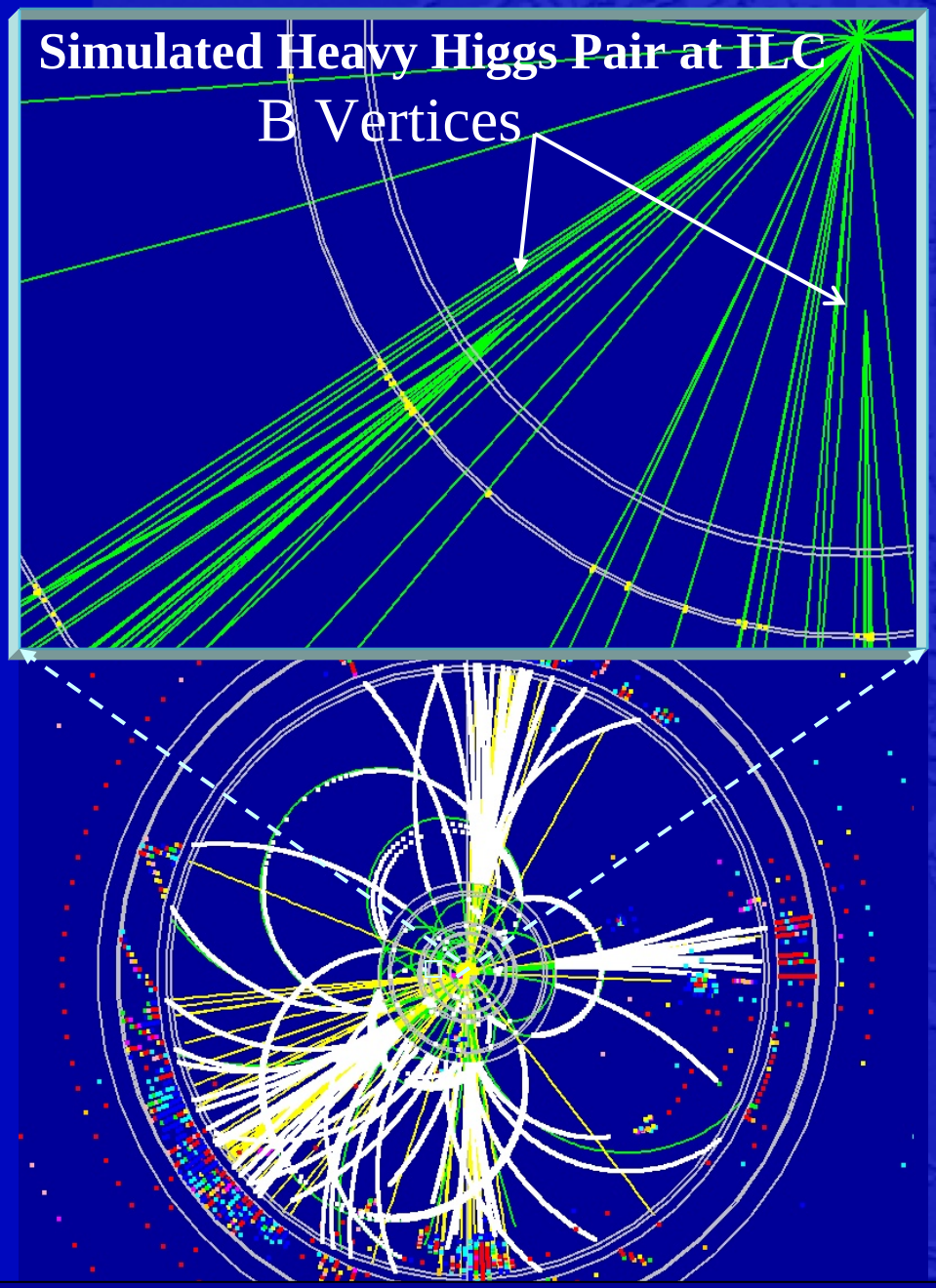
CCDs offer space resolution and thinness but lack readout speed and radiation tolerance

Hybrid pixels have fast readout and are rad-hard but are limited by thickness and pixel size

ILC offers opportunity for monolithic pixel detectors of new concepts: CMOS sensors, DEPFETs, SOI sensors, ...

ILC Technology choice makes important investigating designs beyond CCDs

Comparison of Tracking Performance Targets



Extrapolation to Collision Point

$\sigma_{ip} = a \oplus b / p_t$	a (μm)	b (μm GeV)
LEP	25	70
SLD	8	33
LHC	12	70
RHIC II	14	12
LC	**5**	**8**

Momentum

$\delta p / p^2 GeV^{-1}$	TPC Only	All Tracker
LEP	$1.2\ 10^{-3}$	$5\ 10^{-4}$
LHC	--	$2\ 10^{-4}$
LC	**$1.5\ 10^{-4}$**	**$6\ 10^{-5}$**

Si detectors paradigm for high precision tracking

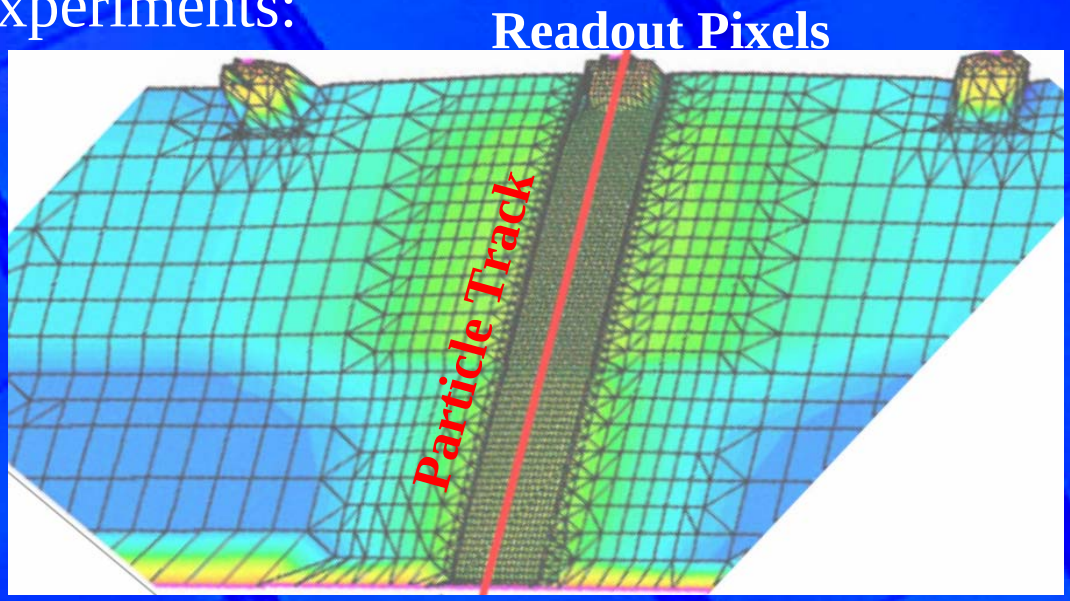
Pixel design to provide unambiguous 3D points along particle tracks

Trend in Detector-Electronics Integration:
maximum of **functions on Chip** for minimum System Noise
and Material burden requires small feature size

Integration of pixel sensors and electronics into Monolithic detectors solution for achieving high density read-out in small active cells

Novel Monolithic CMOS Pixel sensors

from Digital Cameras to Accelerator Experiments:



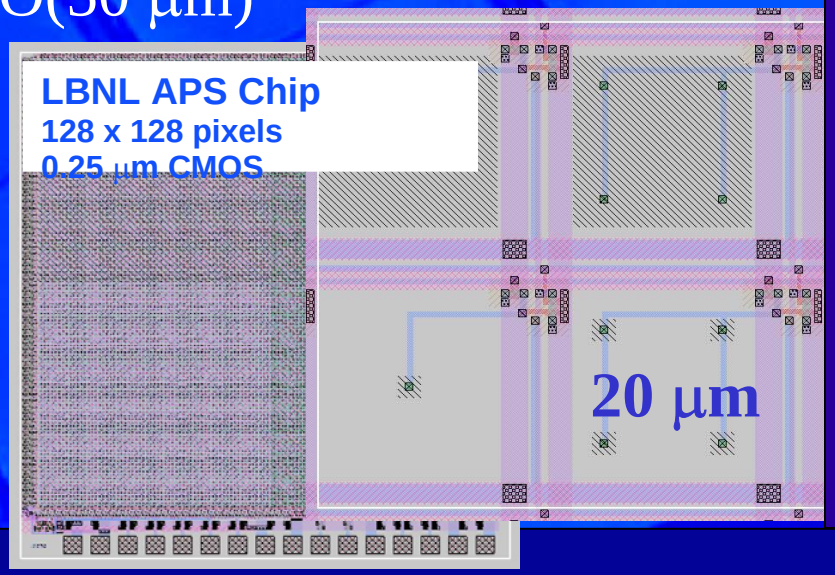
Combine signal process on detector chip: pioneering experience at IReS, LBNL has provided proof of concept:

Fabrication process: industry standard, cost effective, easily available

CMOS sensors offer **excellent single point resolution** O(1 μm), good radiation tolerance and **minimal thickness** O(50 μm)

Now need to develop into smart sensors with fast read-out capability and data reduction implemented on chip:

Important interplay with applications beyond boundaries of particle physics (medical imaging, electron microscopy, astronomy, ...)



CMOS Pixel Sensors LDRD

CMOS Monolithic Pixel program for the ILC approved under the Laboratory-directed R&D (LDRD) program for 3 years (FY05-07)

Project funding covers setting up a dedicated Si pixel detector test facility, IC designers, foundry submissions, salaries for one postdoc and visitors

Pursue R&D to achieve improved charge collection capability, noise suppression, fast read-out and data sparsification:

Implement **active reset functionality**:
- reduce kTC noise
- reduce fixed pattern noise

Evaluate **CMOS imager technology**:
- thick epi-layer
- reduced leakage current

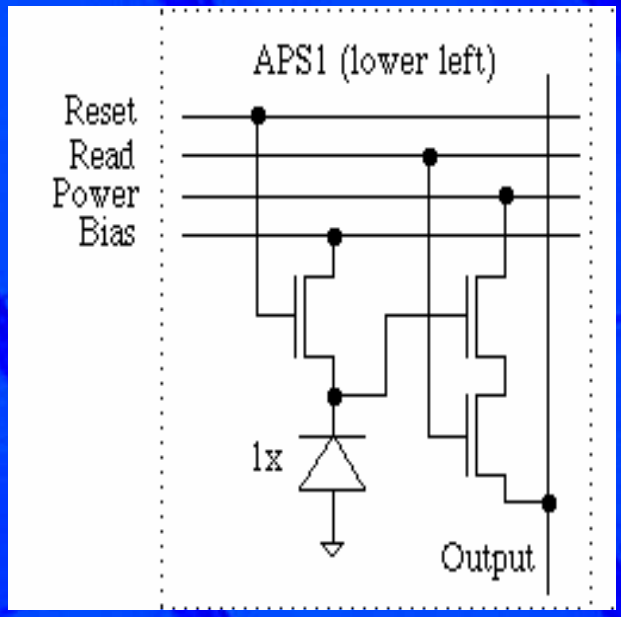
Define sensor specs based on full simulation of benchmark reactions including machine induced backgrounds and material effects;
Develop engineered design of Vertex Tracker based on CMOS sensors.

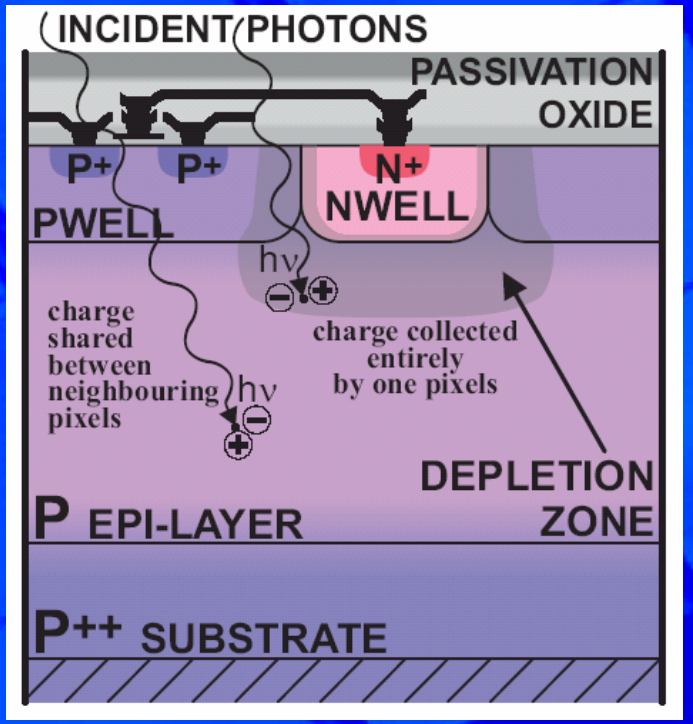
CMOS Sensor R&D

CMOS pixels technology allows to integrate pixel cell and signal processing circuitry on single substrate;

Signal generated by charge carriers created in thin moderately-doped and undepleted epitaxial layer and collected, by thermal diffusion, on n-well p-epi diode

Significant developments by IReS Strasbourg group and new ideas being developed at RAL





Pixel R&D activities at LBNL:

Hybrid Pixel Detector for ATLAS (K. Einsweiler, Physics)

CMOS Pixel R&D for STAR Vertex Upgrade (H. Wieman, Nuclear Science)

CMOS Pixel R&D for Electron Microscopy (P. Denes, Engineering)

CPCCD for experiments at Synchrotron Light sources (P. Denes, Engineering)

ILC LDRD aims at addressing key R&D issues exploiting synergies and opportunities at the interface between different fields and applications.

ILC R&D Lab at LBNL

Setting up new Detector R&D Lab for ILC Activities

Si Pixel Detector
testing facility (LDRD)

TPC VLSI Readout Test Chamber
and ATLAS pixel chip DAQ system

Nano BPM Test setup for
RF Electronics and DAQ

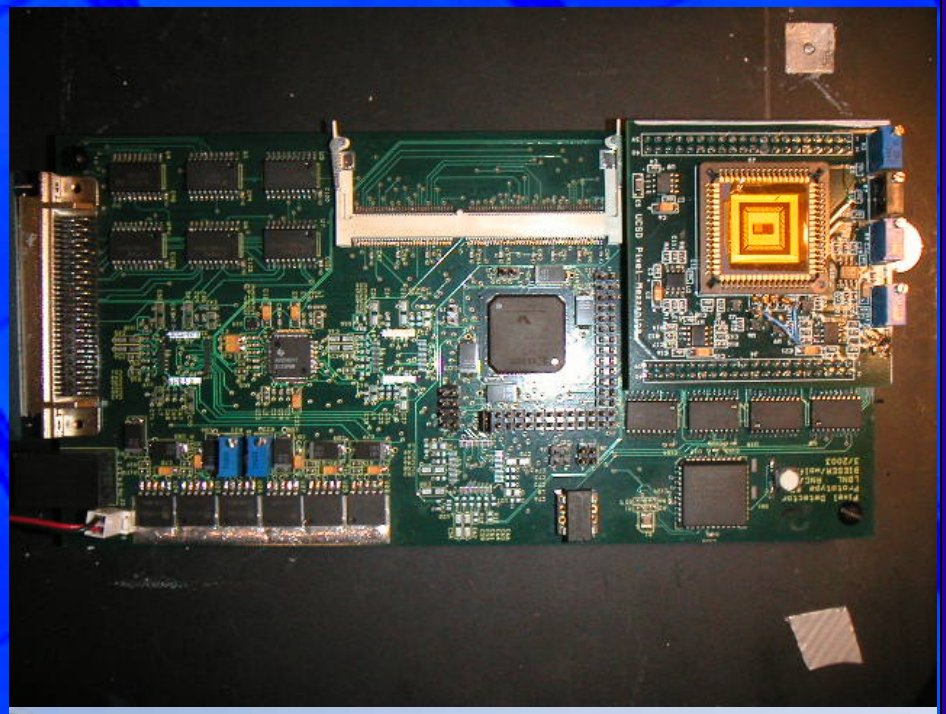
Si Pixel Detector Test Facility

Programmable readout board for driving MIMOSA and pixel test structures

DAQ system based on PC NI card driven by LabView program performing online pixel analysis (CDS, pedestals, rms)

Vibration Isolation Workstation with pneumatic stabilization equipped with high-resolution computer controlled Linear Stages

Photonics Custom Diode Lasers providing 15mW beam focussed to <5µm spot

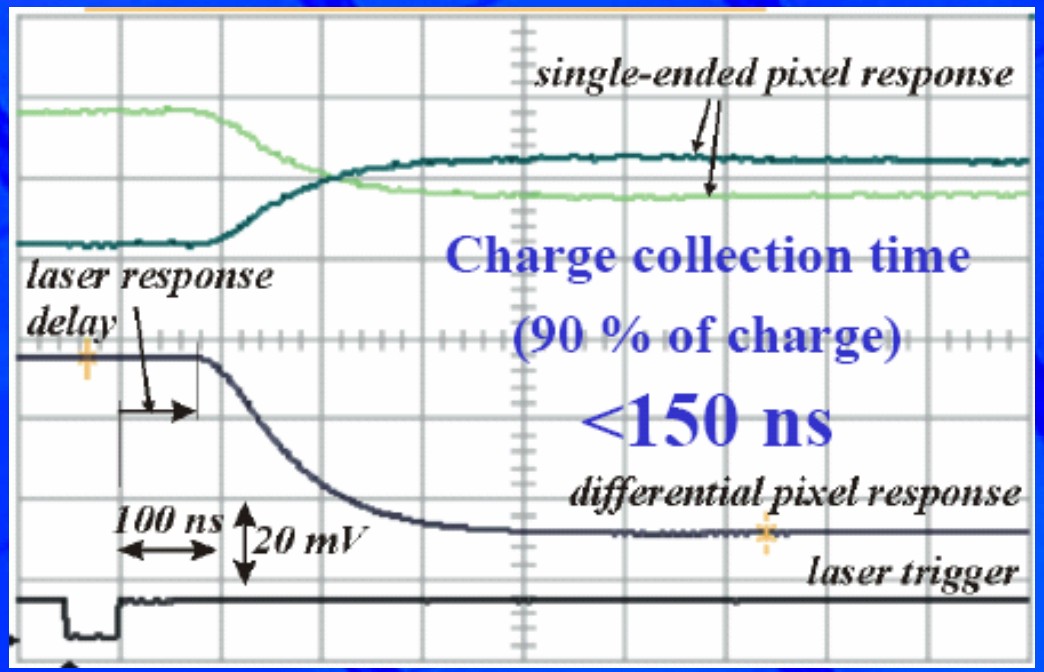


CMOS Sensor R&D

Use laser scan facility to:

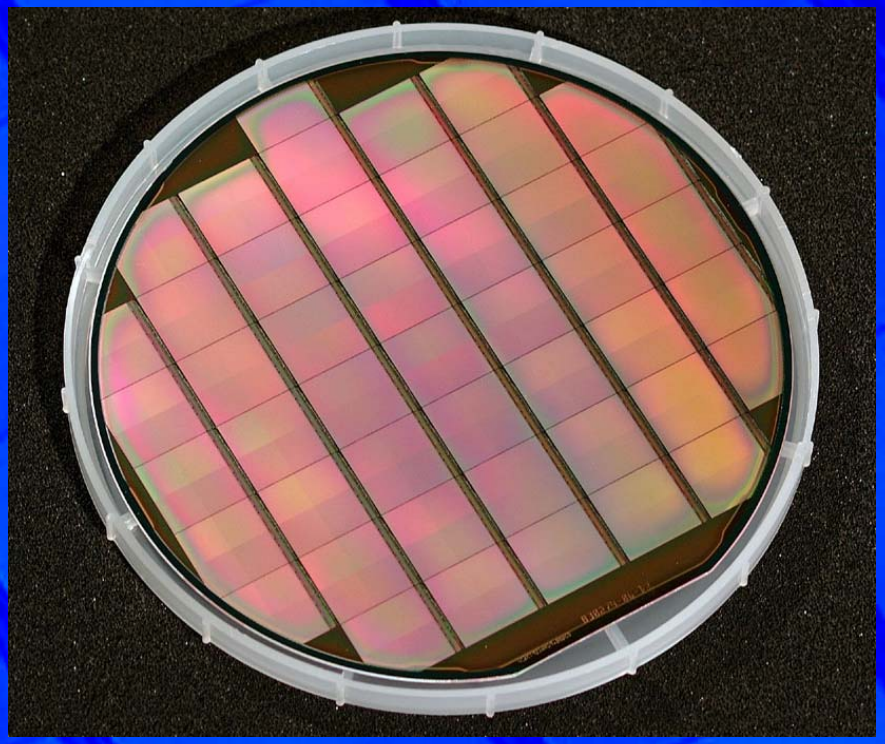
• study charge collection mechanism in pixels of different sizes and designs;

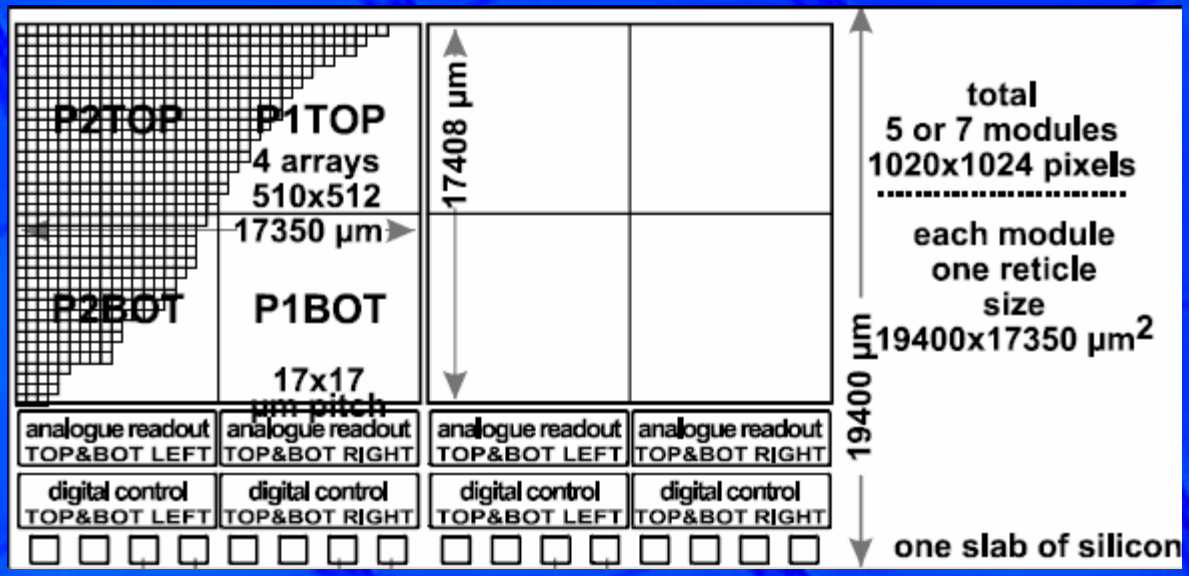
• optimise pixel geometry for point resolution and cluster size;



CMOS Pixel Tests

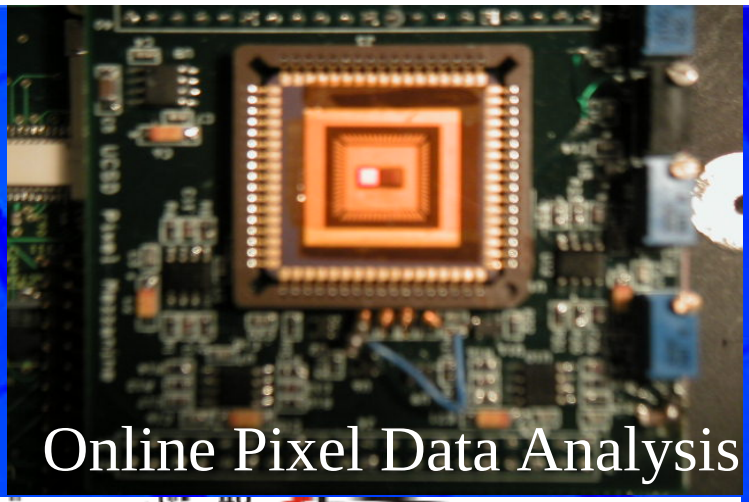
First tests with MIMOSA V chip
0.6 µm CMOS, 14 mm epi-layer
17x17 µm^2 pixels, 4 matrices of 512x512 pixels read-out in parallel
Classic 3-Transistor Scheme



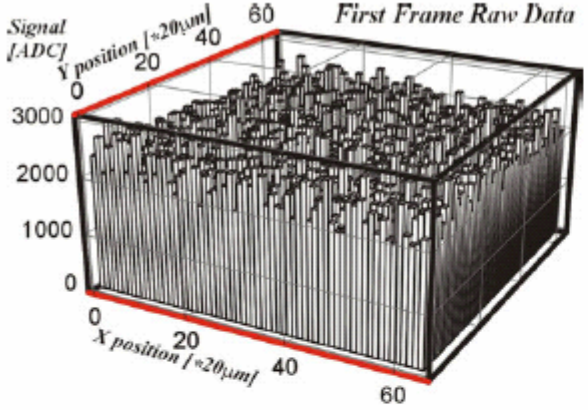


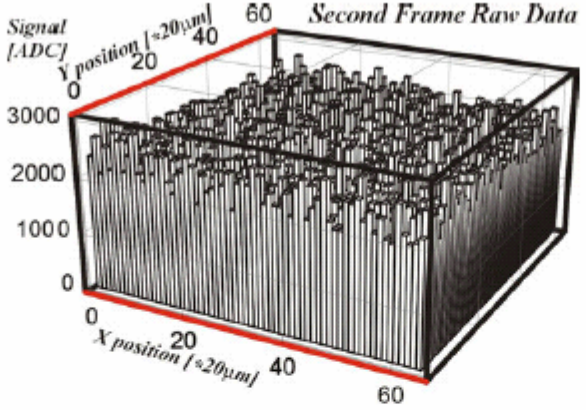
First Results of Mimosa V Tests

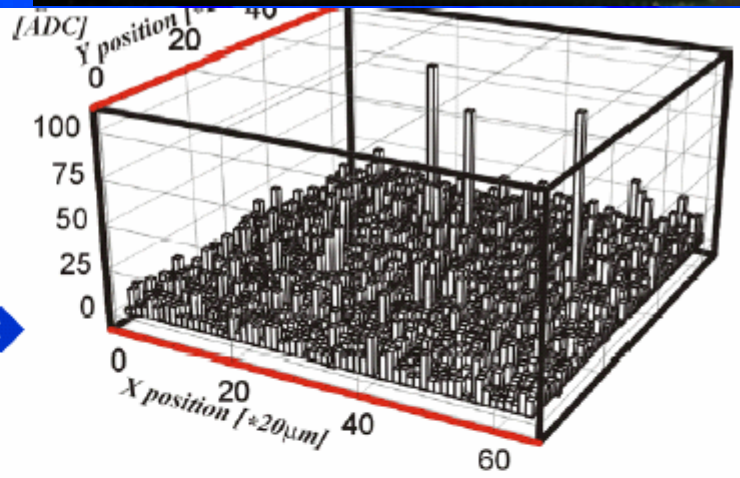
Test performed with ^{55}Fe source
read 2 subsequent frames of 512x128 pixel array
Online CDS, pedestal subtraction, rms calculation



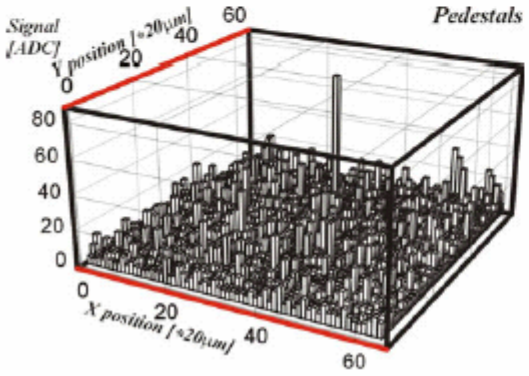
- **Off-line CDS:**



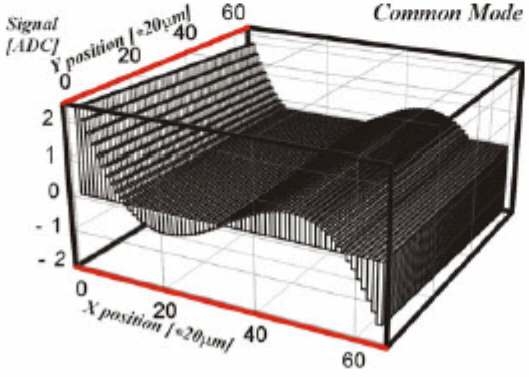


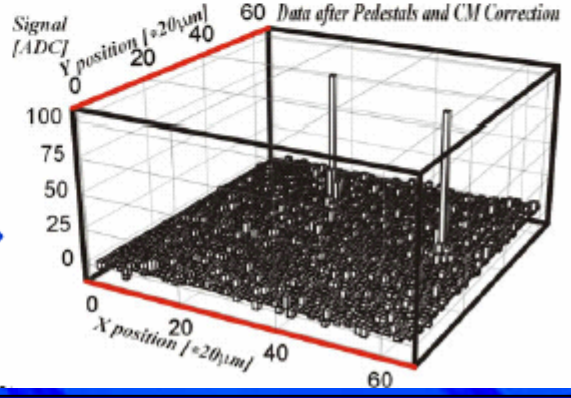


- **CDS Pedestals:**



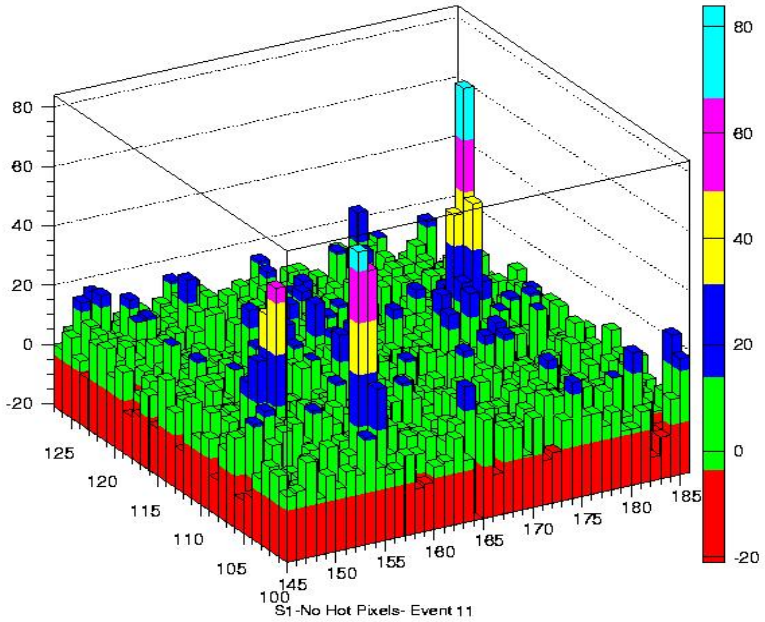
- **Common Mode:**



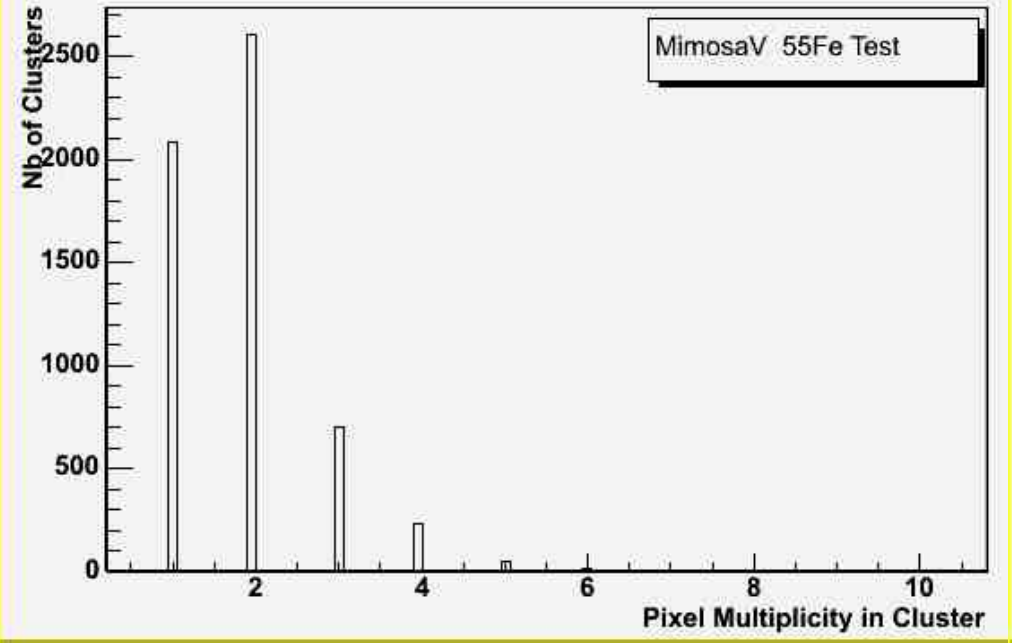


First Results of MIMOSA V Tests

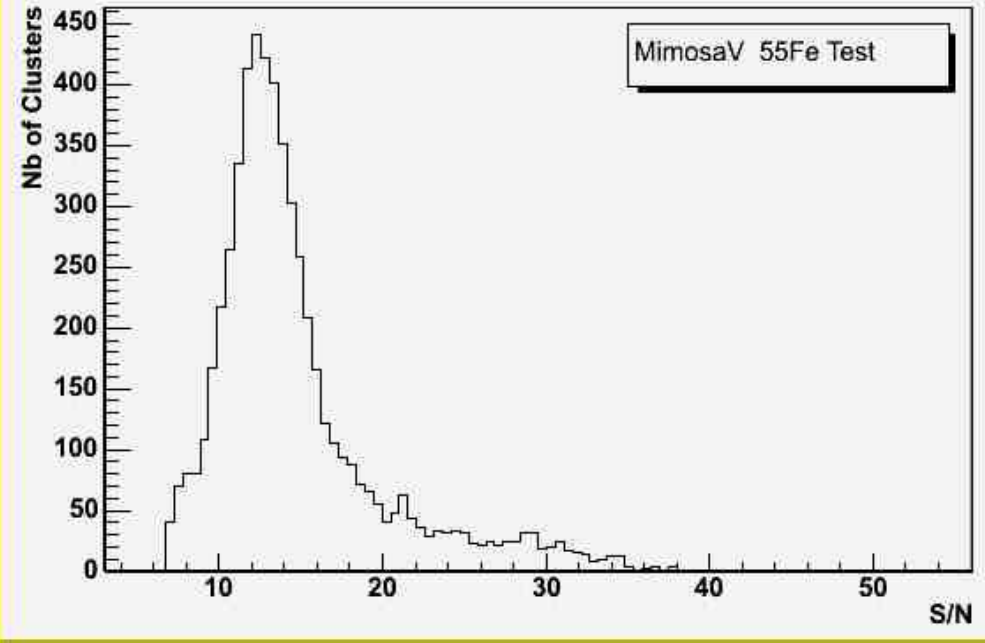
Offline Cluster finding algorithm locating pixels above S/N threshold, finding local maximum and adding neighbouring pixels based on S/N and cluster shape:



Cluster Size



Cluster S/N

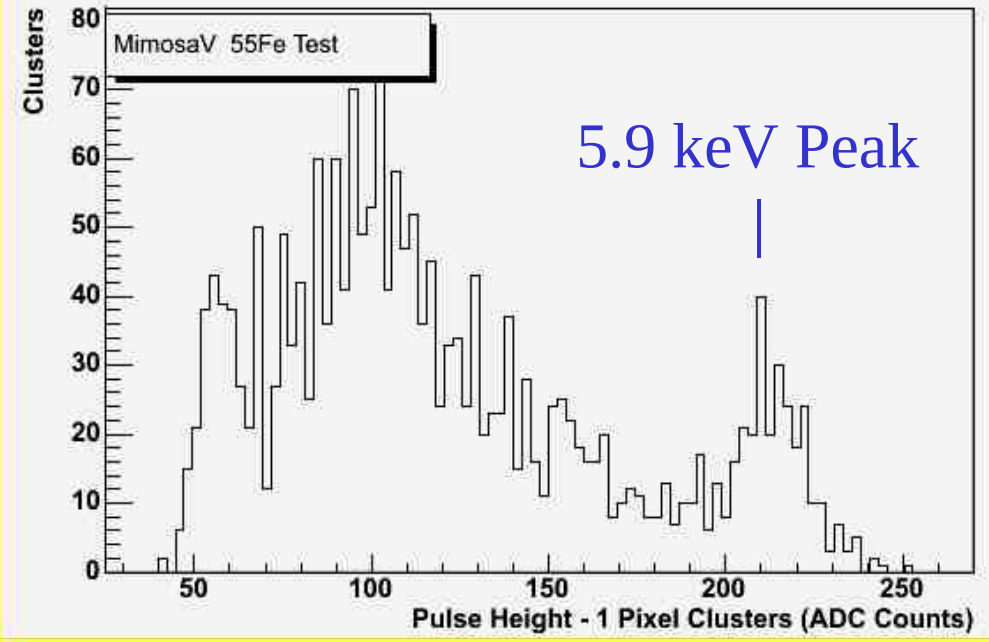


Calibration using ^{55}Fe 5.9 keV peak

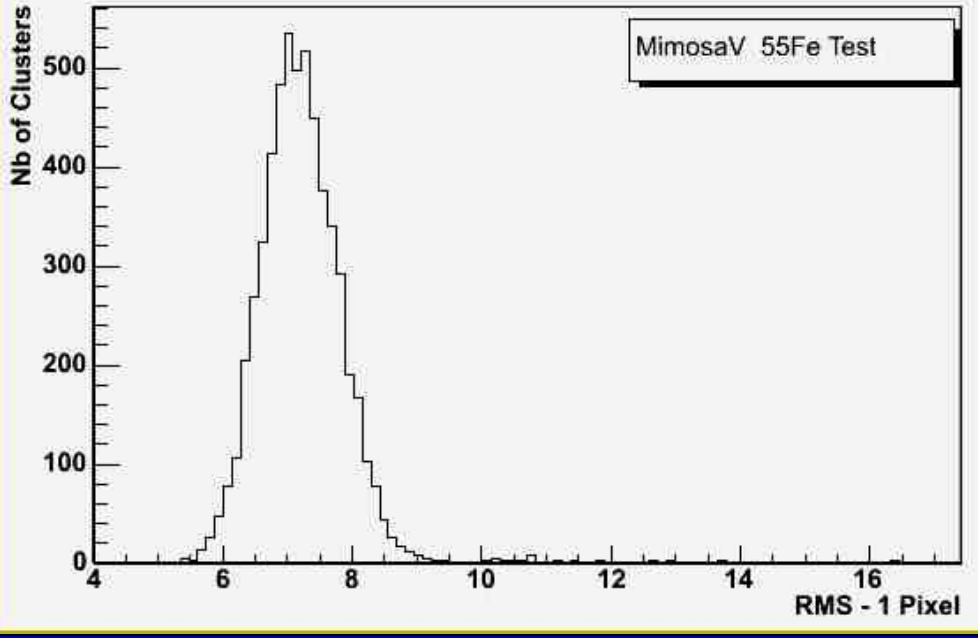
Observe 5.9 keV peak in single pixel clusters

Cluster Multiplicity	**1.98**
ENC Noise	**40.**
S/N	**16.**

Pulse Height 1-Pixel Clusters



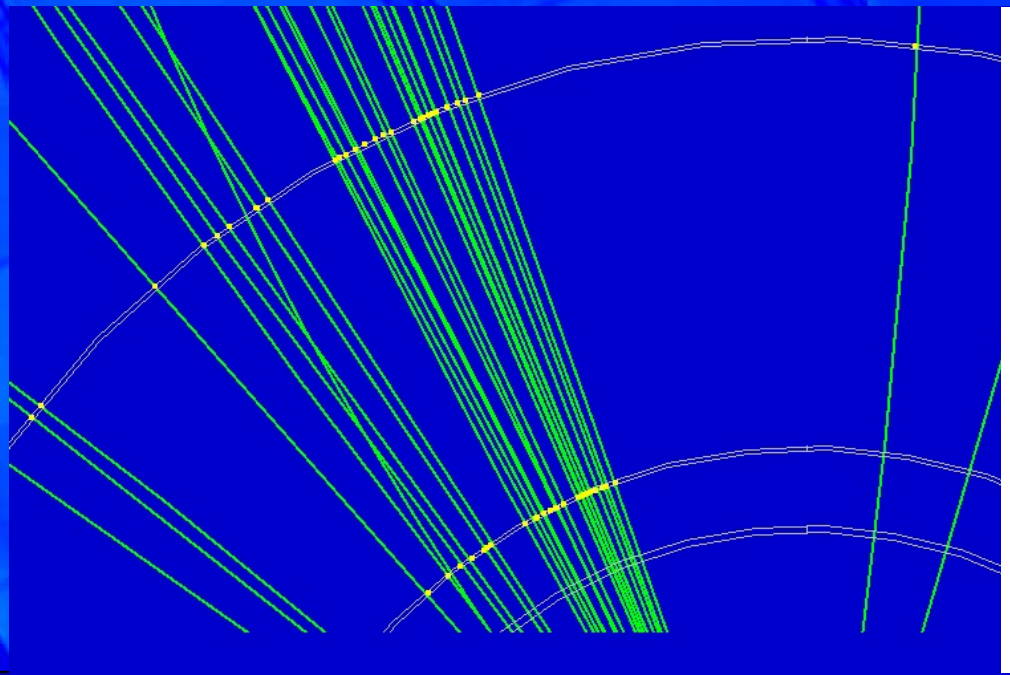
Pixel RMS

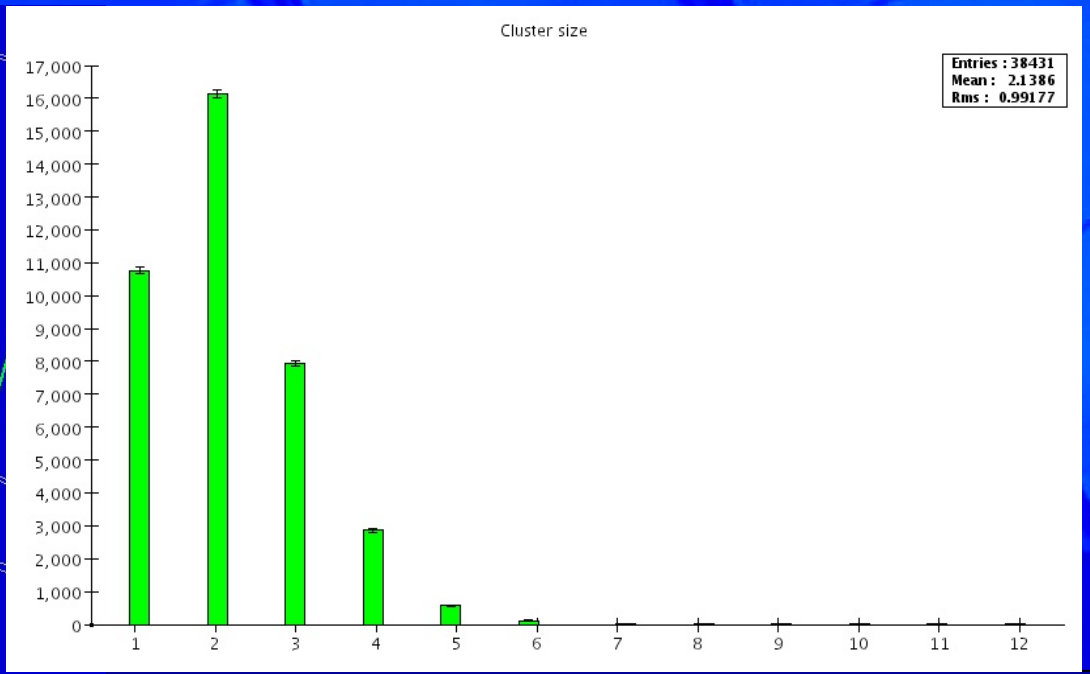


Simulation studies

Study two-track separation and cluster merging using pixel response from lab test and CERN test beam results (MIMOSA V and IX) in collaboration with Strasbourg

Tune and customize **hep.lcd.CcdSim** digitisation code written in Java by N. Sinev to CMOS pixel response and perform study on selected benchmark processes:





CMOS Sensor R&D

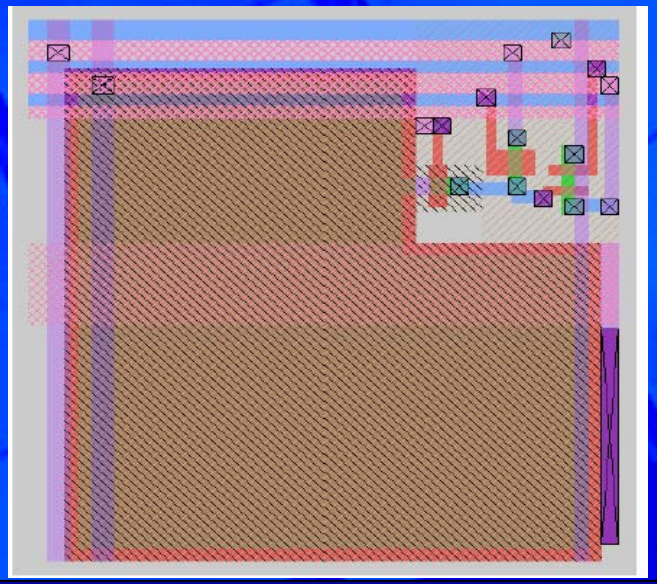
First submission planned for March 05:

simple test structures with 3T- and 4T- pixels of different size
AMS 0.35μm CMOS-OPTO processing through MOSIS
14μm (20μm optional) epi layer, low dark current (<40nA/mm^2)

- Characterise structure response using laser scans and ^{55}Fe source

Second submission of more advanced sensor, including on-chip ADCs and optimised pixel geometry by end 05

Concurrently investigate
PhotoGate design to:
- improve signal collection
- rapid refresh to avod pile-up
- on-chip correlated double sampling for noise suppression



CMOS Sensor R&D

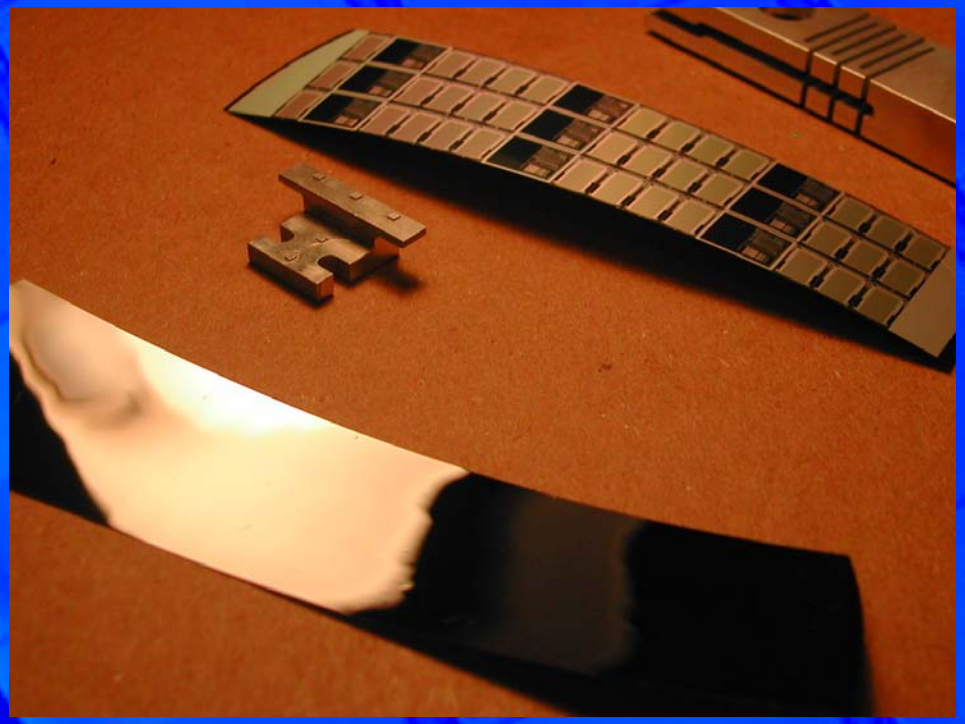
At ILC beamstrahlung gives $5e^{-}$ cm^{-2} BX^{-1} at 0.5 TeV:
need to readout layer 1+2 in 25-50μs and layer 3-5 in 100-200μs

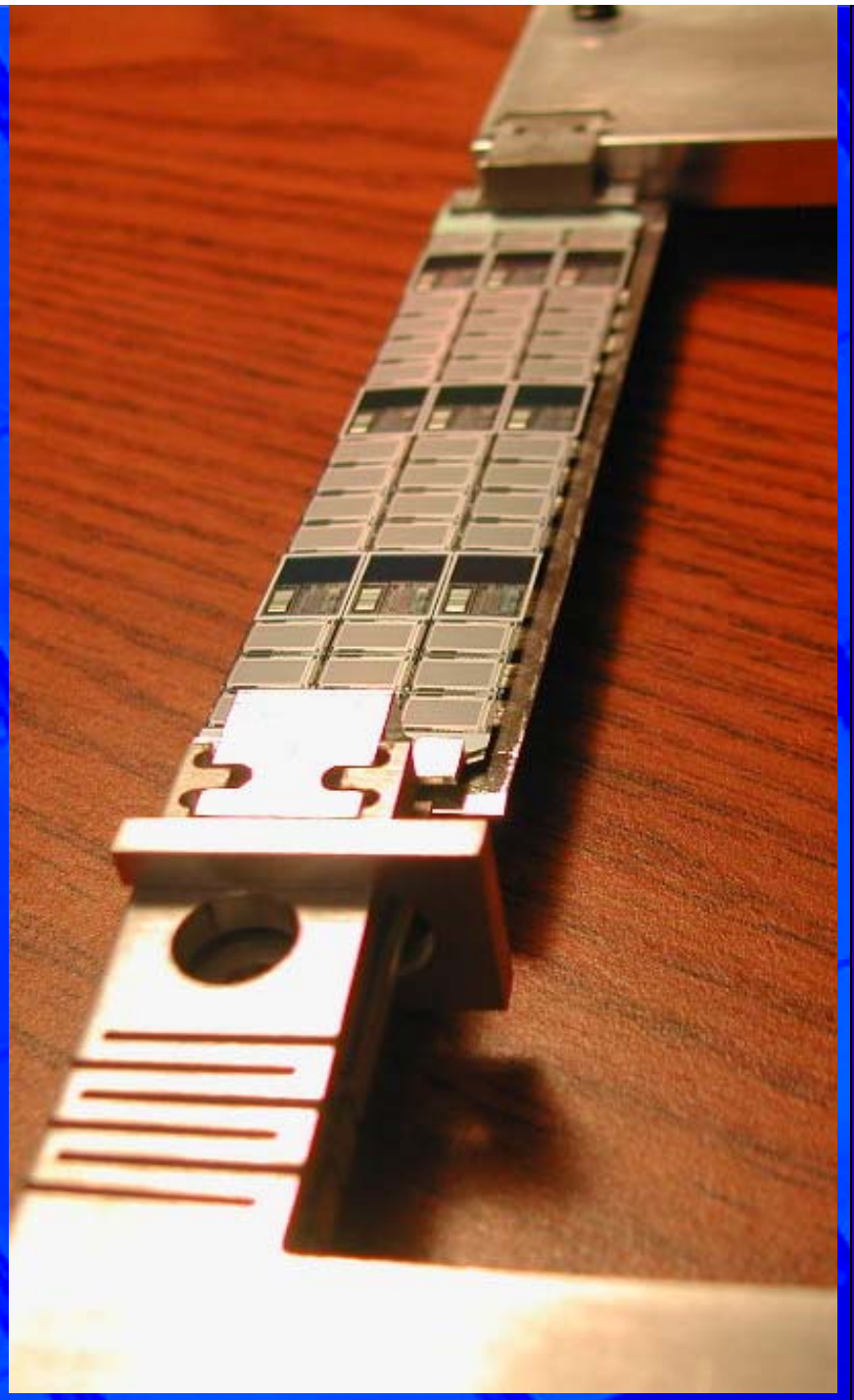
- development of on-chip zero suppression for CMOS pixels:
study optimal definition of RoI in offline analysis, develop amplifiers, low-offset discriminators, individual discriminator level setting,
- on pixel charge storage for CDS, multiple scans during bunch train;
- need to develop readout scheme robust against RF pick-up
- design and submission of test chip with active reset
- develop specialised circuit for baseline subtraction

Sensor Backthinning

First tests of MIMOSA chip backthinning by LBNL STAR group successful to 50μm

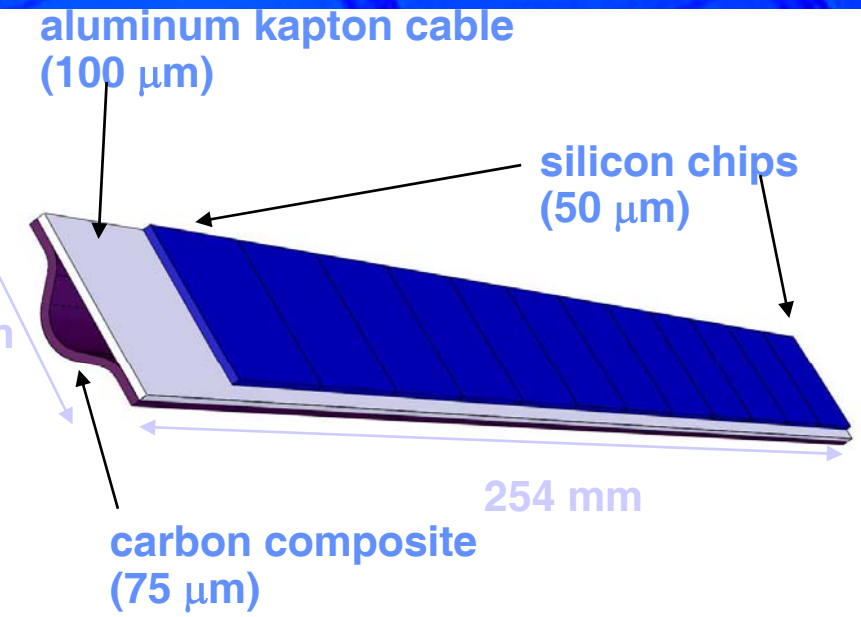
Plan to perform repeated essays of sensor backthinning from US vendors and functionality tests

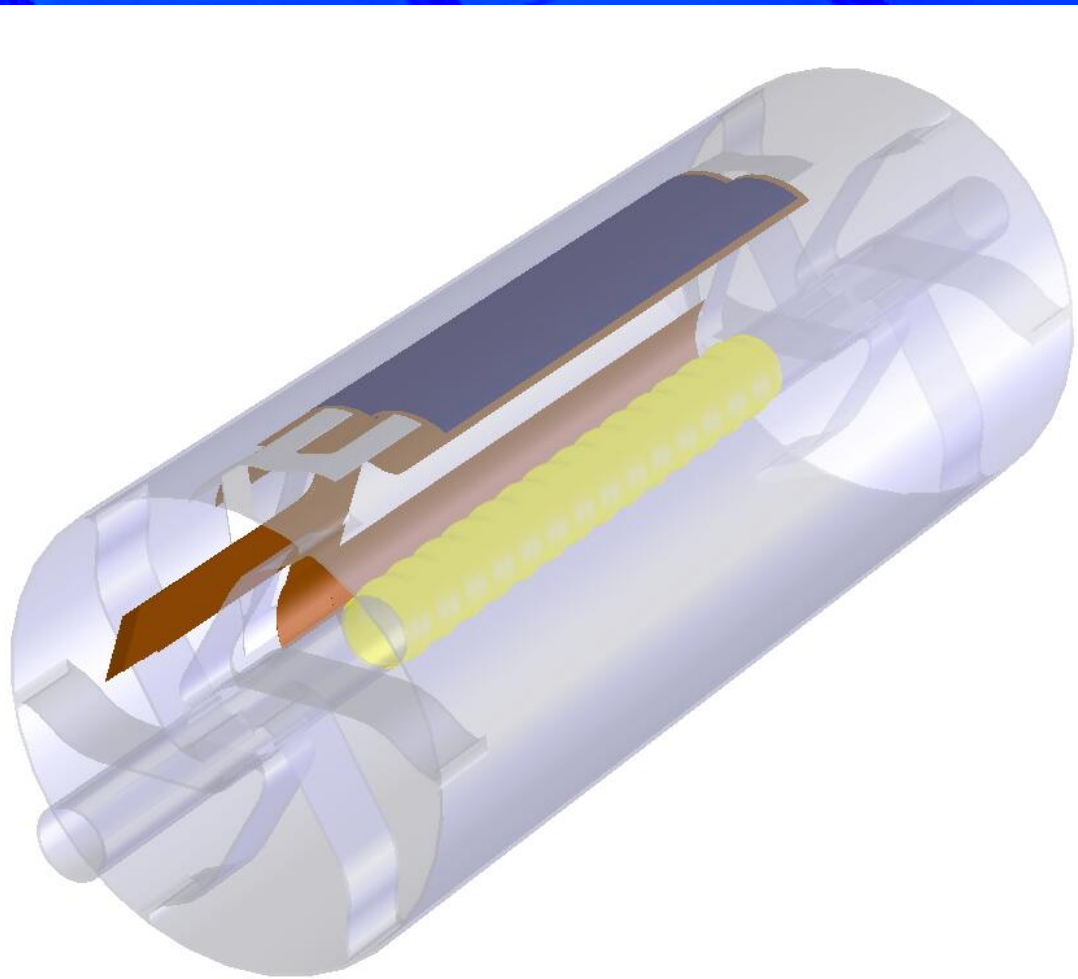




Vertex Tracker Engineering Design

Important experience being accumulated with STAR Vertex Detector to be transferred to engineering design for ILC Vertex Tracker





Nano-scale Microelectronics

0.13 μm CMOS process current industrial standard: smaller feature size

- provides **higher level of integration**
- **more functionalities** for cell readout
  (x 4 circuit density compared to state-of-the-art 0.25 μm process)

- Thin oxyde **increases rad-tolerance** instrumental to high-lumi SLHC

0.13 μm CMOS technology of choice for next generation detectors, but along with many attractive feature come new challenges to be addressed in prototyping of digital and analog circuit blocks to be characterised in Lab.

LDRD program to **set the foundation** for development of **fully integrated electronics** for next generation of tracking detectors at particle colliders

LDRD Project Plan

LDRD based on synergy of R&D activities aimed at different applications:

- share common technological basis
- bridge from end of construction for state-of-art detectors for LHC and RHIC to advanced R&D within ILC Collaborations

R&D program open to Universities and other Labs:

Post-Docs and UCB GSI, shared with current programs, and UCB URAPSs to train young physicists in time for future Experiments;

UCB Faculty and LBNL Staff
M. Battaglia (PI), G. Abrams, P. Denes, L. Greiner, H. Matis, H. Wieman

UC Berkeley students
L. Ferrerosa, A. Gallardo, M. Tuchscher, M. Reddick

Collaborating Institutions:
UC Irvine, UC Davis, IReS Strasbourg