SiD Electronic Concepts

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Si-W Calorimeter Concept

Transverse Segmentation ~5mm
30 Logitudinal Samples
Energy Resolution ~15%/E^{1/2}
Electronics requirements

- **Signals**
  - <2000 e noise
  - Require MIPs with S/N > 7
  - Max. signal 2500 MIPs (5mm pixels)
- **Capacitance**
  - Pixels: 5.7 pF
  - Traces: ~0.8 pF per pixel crossing
  - Crosstalk: 0.8 pF/Gain x Cin < 1%
- **Resistance**
  - 300 ohm max
- **Power**
  - < 40 mW/wafer ⇒ power cycling
    (An important LC feature!)
- Provide fully digitized outputs of charge and time on one ASIC for every wafer.
Multi-Layer G-10

Wire Bond

Readout Chip

Bump Bonds

Silicon Wafer

Wafer and readout chip

16 traces [maximum] from pixels to a typical bump pad row
Each trace 0.006 wide

6.20 +/- 0.04

5 mm

17.50 +/- 0.04

Unit: mm

Bump Pad Array, v2.1

R. Frey

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Traces to bump pads, typical
Conceptual Design of W-SI Front-End ASIC

There is an 18 page technical document, now in its 4th major revision for register assignments, etc for the cold bunch structure.
Si-W Pixel Analog Section

Simplified Timing:

There are ~3000 bunches separated by ~300 ns in a train, and trains are separated by ~200 ns.

Say a signal above event threshold happens at bunch n and time T0.
The Event discriminator triggers in ~100 ns and removes reset and strobes the Timing Latch (12 bits), Range latch (1 bit) and Event Counter (5 bits).
The Range discriminator triggers in ~100 ns if the signal exceeds the Range Threshold.
When the glitch from the Range switch has had time to settle, Track connects the sample capacitor to the amplifier output. (~150 ns).
The Track signal opens the switch isolating the sample capacitor at T0 + 1 micro s. At this time, the amplitude of the signal at T0 is held on the Sample Capacitor.
Reset is asserted (synchronized to the bunch clock). Note that the second capacitor is reset at startup and following an event, while the high gain (small) capacitor is reset each bunch crossing (except while processing an event).
The system is ready for another signal in ~1 micros.
After the bunch train, the capacitor charge is measured by a Wilkinson converter.
Pulse “Shaping”

- **Take full advantage of synchronous bunch structure:**
  - Reset (clamp) feedback cap before bunch arrival. This is equivalent to double correlated sampling, except that the “before” measurement is forced to zero. This takes out low frequency noise and any integrated excursions of the amplifier.
  - Integration time constant will be 0.5 – 1 µsec. Sample *synchronously* at 2 – 3 integration time constants.
  - Time from reset 1 – 3 µsec, which is equivalent to a 1 – 3 µsec differentiation.

- **Noise:** ~1000 e⁻ for ~ 20 pF. (100 µA through input FET).
Data transmission is by pairs on a motherboard at 20 Mbits/sec. The ROC's do not suppress data, so each ROC has 1024 pixels x 4 measurements/pixel x (12 amplitude + 12 time + 1 range) = 12.8 Kbytes. So one ROC takes 5.12 ms to readout; with overhead assume 6 ms. Assume 8 ROC are simultaneously active, then time to readout board of 100 is ~75 ms, which is ok wrt 200 ms intertrain period.
Tracker Pixel Analog Section

1 of 2048 pixels

Simplified Timing:

There are ~ 3000 bunches separated by ~300 ns in a train, and trains are separated by ~200 ms.

Say a signal above event threshold happens at bunch n and time T0. The Event discriminator triggers in ~100 ns and removes resets and strobes the Timing Latch (12 bit) and Event Counter (5 bits).

Track connects the sample capacitor to the amplifier output (~150 ns).

The Track signal opens the switch isolating the sample capacitor at T0 + 1 micro s. At this time, the amplitude of the signal at T0 is held on the Sample Capacitor.

Reset is asserted (synchronized to the bunch clock).

The system is ready for another signal in ~1.2 microsec.

After the bunch train, the capacitor charge is measured by a Wilkinson converter.
EXO DAQ Architecture

Data Flow - ~ 4 Mb/train from backgrounds...
Comments

• The basic architecture should work with all the low occupancy sub-systems.
  - Including Tracker, EmCal, HCal, and muon system.
  - It does not address VXD issues - presumably CMOS to be developed - or the completely occupied Very Forward Calorimeters.
  - A variant might work in the forward regions of the tracker and calorimeters.
• The cost of a mask set is high, so development will be with (probably) 8 x 8 subsets instead of the 32 x 32 array.
• The unit cost of a large number of chips seems fine - $40.
• Substantial design and simulation is done on EMCal Readout chip.
• ~No work done on anything else.