a few selected calorimeter-related items from Paris LCWS

Ray Frey
LCD May 20, 2004

Items of special interest (to me) …

• warm vs cold
  ▪ backgrounds
    ▪ Tim (2 weeks ago)
    ▪ K. Desch
  ▪ timing
  ▪ forward cal (last week)
• revisiting global detector design
• particle flow
• Si/W ECal
Warm or Cold ??

Implications on detector design

(my opinion: small effects )

- energy spread
- bunch timing structure
- crossing angle
Timing is good

**Warm detector concern:**
Pileup of $\gamma\gamma \rightarrow$ hadrons over bx train

192 bx pileup
(56 Hadronic Events/Train)

3 bx pileup (5ns)

Si/W ECAL Timing $\sim$ 1 ns
Timing and Bunch Structure

- Warm–Cold Differences and Possible Implications
- Background Characteristics
- Hadronic Background: Impact on Physics

Klaus Desch, University of Hamburg

LCWS04, Paris, 20/04/04
What can be achieved?

Tracking:
Studies indicate 2-5 ns track timing possible in principle for TPC and Si
Detailed time-dependent simulation needed – non-trivial

Calorimetry (most important in central detector, many neutrals):
With electronics inside Si-W calorimeter 5ns for single cells achievable in SLAC design
Averaging over 30 hits: $5 \text{ ns} / \sqrt{30} = 1 \text{ ns}$ (Jaros, Frey)

Concerns:
- Distribute o(GHz) clock over a large detector
- Timing calibration for o($10^8$) cells (o($10^5$) r/o chips) to ns precision
- Cluster finding to do the averaging – need detailed time-dependent simulation
- Charged particles in endcap: time-of-flight correction (loopers!)
Preliminary Summary

Integrating the hadronic background from more than a few bunch-crossings has a sizeable impact on the physics performance.

America, Asian, and European studies agree.

At NLC, a bunch tagging of few ns is needed to become comparable to the TESLA situation.

→ R&D on detector timing is vital for warm technology.

→ Timing capability adds complexity – how much?
Revisiting global detector design

• Special parallel session on global design
• Brient:
  ▪ Reconsidering TESLA TDR detector
  ▪ Merging SiD and TDR

• Keeping the current R&D consortia (eg CALICE)

• Two leading detector models: TDR and SiD
• How to “internationalize” the involvements
Two detector options today ... SD vs TDR [*]

<table>
<thead>
<tr>
<th>TRACKER</th>
<th>SD</th>
<th>TDR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon tracker</td>
<td>Digital / Tile AHCAL</td>
<td></td>
</tr>
<tr>
<td>TPC and Si envelope</td>
<td>Digital / Tile AHCAL</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CALORIMETRY</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>ECAL</td>
<td>Digital (RPC, GEM,..)</td>
<td>tungsten-silicon both options</td>
</tr>
<tr>
<td>HCAL</td>
<td>Digital / Tile AHCAL</td>
<td>Digital / Tile AHCAL</td>
</tr>
</tbody>
</table>

Partly the same people
The 2 options following J. Jaros

Silicon area TDR ~ 2.6
Silicon area SiD

The only (main) justification for the SD detector ??!!

### ECAL

- $R_{\text{min}}$ barrel (m):
  - TESLA: 1.68
  - SD: 1.27

### HCAL

- $R_{\text{min}}$ barrel:
  - TESLA: 1.91
  - SD: 1.43
  - LD: 2.50
  - JLC: 2.0

### Table

<table>
<thead>
<tr>
<th></th>
<th>TESLA</th>
<th>SD</th>
<th>LD</th>
<th>JLC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tracker type</td>
<td>TPC</td>
<td>Silicon</td>
<td>TPC</td>
<td>Jet-cell drift</td>
</tr>
<tr>
<td>Type</td>
<td>Si pad/W</td>
<td>Si pad/W</td>
<td>scint. tile/Pb</td>
<td>scint. tile/Pb</td>
</tr>
<tr>
<td>Sampling</td>
<td>$30 \times 0.4 X_0$</td>
<td>$30 \times 0.71 X_0$</td>
<td>$40 \times 0.71 X_0$</td>
<td>$\frac{30 \times 0.71 X_0}{2}$</td>
</tr>
<tr>
<td>Gaps (active) (mm)</td>
<td>2.5 (0.5 Si)</td>
<td>2.5 (0.3 Si)</td>
<td>1 (scint.)</td>
<td>1 (scint.)</td>
</tr>
<tr>
<td>Long readouts</td>
<td>40</td>
<td>30</td>
<td>10</td>
<td>3</td>
</tr>
<tr>
<td>Trans. seg. (cm)</td>
<td>$\approx 1$</td>
<td>0.5</td>
<td>5.2</td>
<td>144</td>
</tr>
<tr>
<td>Channels ($\times 10^6$)</td>
<td>32000</td>
<td>500000</td>
<td>135</td>
<td>5</td>
</tr>
<tr>
<td>$Z_{\text{min}}$ endcap (m)</td>
<td>2.8</td>
<td>1.7</td>
<td>3.0</td>
<td>1.9</td>
</tr>
</tbody>
</table>

### Notes

- Silicon area TDR ~ 2.6
- Silicon area SiD
- The only (main) justification for the SD detector ??!!
Reason for 2.50m for the TPC length
  • Covering at low angle?

Reason for the TPC radius of 1.60m
  • Single track resolution?
  • Separability?

Reason for 1.70m for the ECAL radius
  • TPC radius + 10cm
  • Compact ECAL to save space for HCAL inside coil

Reducing the external radius of the TPC (reduce the cost of the overall detector)
  • Impact on the momentum resolution?
  • if needed a precise point outside TPC can be added??
  • what about the charged-neutral separation??

Tracker size

ECAL size
Is it so different?
At least, there is a good agreement on the global geometry
The ECAL internal radius

For SD geometry, there is an average of \(~65\text{GeV}\) of photons closer than 2.5 cm versus \(~20\text{ GeV}\) for the TDR geometry.

\[e^+e^- \rightarrow ZH \rightarrow \text{jets} \text{ at } \sqrt{s} = 500 \text{ GeV}\]
Energy per event for photons closer than 2.5 cm from a charged track at the ECAL entrance.

Example here with $B=4$T, $R=170$cm.

The average is here.

What for different physics process

$\sqrt{s} = 800$ GeV

$e^+e^- \rightarrow WW$ at $\sqrt{s} = 800$ GeV

Efficiency of reconstructing photons close to ch. track ($D<R_m$) is $<<100\%$.
Variation with the ECAL endcap entrance

Internal radius fixed at 1.50 m and B=4T

We define Rm at 2cm

SD Value

W W final state at 800 GeV

When going to 1 TeV

Fraction of photons energy at D<Rm

Length of the TPC

Distance of the ECAL endcap
Variation with the internal ECAL radius

Z endcap at 2.00 m and B=4T

Fraction of photons energy at $D < R_m$

Internal radius of the ECAL cm

SD Value

W W final state at 1 TeV

SD Values Rint=125, Zec=170 and B=5T
Is it possible reducing the calor. cost AND saving the EFLOW performances?

ECFA Krakow Sept. 2001

Curves ISOCOST(area) versus SiD

Possible Region Of Interest

TESLA TDR

Internal radius of the ECAL

Length of the ECAL barrel

AE( component in jet) GeV

SiD detector

20 layers

25 layers

30 layers

20 LAYERS

40 LAYERS

+11%

Software improvement

Tesla Design Report

J-C. BRIENT (LLR)

J-C Brient- LCWS 2004
For the TDR type of detector \((R=170\,\text{cm and} \, 4\,\text{T})\)

14\% of the events have more than 50 \text{GeV} in the difficult region.

For the SiD detector \((R=125\,\text{cm and} \, 5\,\text{T})\)

32\% of the events have more than 50 \text{GeV} in the difficult region.

Due to the large value of the WW cross section, Any signal in jets could be overflowed ?!

For the photon(s) reconstruction, the ECAL radius and Z endcap is much more important !!!

Impact on the jets to be quantified ?

To reduce the ECAL cost,

Playing with layers number is more efficient and less penalizing for the performances on jet, \(\tau\), \ldots ?!

A new detector proposal

\(~20-25\) layers ECAL at \(R\approx 1.55\,\text{m} \?? Z_{\text{ECAL}} \??\)
Tau decays ID is essential for τ ID and polarisation measurement.

<table>
<thead>
<tr>
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<th>Jet mass &lt; 0.2</th>
<th>Jet mass in 0.2-2</th>
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<tbody>
<tr>
<td>$\tau \rightarrow \pi\nu$</td>
<td>82%</td>
<td>17%</td>
</tr>
<tr>
<td>$\tau \rightarrow \rho\nu$</td>
<td>2%</td>
<td>90%</td>
</tr>
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</table>

$\tau(250 \text{ GeV}) \rightarrow \rho\nu$

Why “continuous” readout is needed.

Looking along the charged track in the first 4 X0.

Looking along the charged track in 5-12 X0.
 Tau decays ID is essential for τ ID and polarization measurement

\[ \tau(250 \text{ GeV}) \rightarrow \rho \nu \]

True for TDR geometry for smaller detector??

Why "continuous" readout is needed

Looking along the charged track in the first 4 X0

Looking along the charged track in 5-12 X0

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<td>τ → πν, ρν</td>
<td>90%</td>
</tr>
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<td>17%</td>
</tr>
<tr>
<td>τ → πν</td>
<td>82%</td>
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</table>
Summary of the ECAL change vs TDR

- VFE inside for the ECAL, alveoli thinner, better eff. Molière radius
- For the simulation, I propose to use 30 layers to be consistent with the SiD ECAL and with the prototype in construction

Changing the general geometry

- VFE inside for the HCAL (Si-PM, or digital readout for DHCAL)
  - NO SPACE for fibbers in overlap !!! 😊
  - NEW distance TPC-ECAL in endcap !!!!

New way of the ECAL readout

VFE (with ADC?) send each BX to DAQ board (with/without ADC)
DAQ-ADC board digitise, store in digital memory, MUX to optical link

- VFE time occupancy is about 1/200 for TESLA
- VFE On-Off take about 100 μs
  ⇒ Simulation gives ~100μW/channel !!! (source CdlT)

Passive cooling would be sufficient (source JB)

Modify Simulation (better $R_m^{\text{eff}}$

R&D in CALICE ECAL (IN2P3, KNU, MSU) to quantify this passive cooling limit
Other open questions

- Quantitative variation of performances on jet(s) (and impact on physics program) with **TPC size**

- Is there a way to avoid the hole between Forward CAL and ECAL together with the possibility to open the detector?

- A dedicated study of the CALOR endcap geometry

- Using ECAL to seed the high Pt track in the SiD tracker? *a kind of substitute for the large number of points in a TPC*

- FCH (SET?) in silicon device inserted in ECAL CFi frame? **See next slide**

- What is the **number of X0** of the endplate and readout electronics? what is the **distance TPC-ECAL**?
If precise point(s) outside TPC is mandatory

Add alveoli with 2 double side strips without tungsten

- Minimize the thickness/"tracker point"
- Minimize the distance to the ECAL
- Minimize the inter alignment tracker-ECAL and

ASSEMBLING SIMPLICITY

Strips along R\(\Phi\) in the barrel

\[\Delta Z \leq \text{Strip Width}\]
For CALOR. geometry, the TDR detector is not so different from the SD detector, but the size.

The PFlow is very probably more difficult with the SD detector (to be quantified).

The impact on the performances from different TPC size, with/without precise points, etc... has to be QUANTIFY.

May be it is time to begin the second round of detector optimisation

Inter-regional proposal would be VERY WELCOME !!

a proposal at the next LCWS ?
Where to go?

- SiD has the lead for the implementation of SiW as an ECal technology (blatantly biased personal opinion)
- But ignoring cost, the reduced radius of SiD is a disadvantage for performance

- TDR and SiD: save money by reducing the number of layers
  - Need to quantify the performance costs
- For TDR: reduce cost by reducing radius
- For SiD: increase performance by increasing radius

- Does it make sense to work toward a common global concept?
- Decouple this from technological implementation, which can remain on separate paths?
M. Breidenbach, D. Freytag, N. Graf, G. Haller, O. Milgrome

Stanford Linear Accelerator Center

R. Frey, D. Strom

U. Oregon

V. Radeka

Brookhaven National Lab
Concept

Si-W Calorimeter Concept

Transverse Segmentation \(~5\text{mm}\)
30 Logitudnal Samples
Energy Resolution \(~15\%/\sqrt{E}\)
• Dynamically switched $C_f$ (D. Freytag)
  - Much reduced power
    - Large currents in 1st stage only
  - Signals after 1st stage larger
    - $\sim 0.1 \text{ mV} \rightarrow 6.4 \text{ mV}$ for MIP

• Time
  - No 4000e noise floor
  - Can use separate (smaller!) shaping time ($\sim 40 \text{ ns}$)
  - Readout zero-crossing discharge (time expansion)
Electronics design (contd)

• Present design gives:
  Noise = 20-30 e/pF
• $C_{in} = \text{pixel} + \text{traces} + \text{amplifier}$
  \[5.7\text{pF} + 12\text{pF} + 10\text{pF} \approx 30 \text{ pF}\]
  \[\Rightarrow \text{Noise} \approx 1000 \text{ e} \quad (\text{MIP is 24000 e})\]

• Timing: \(~5 \text{ ns per MIP per hit}\)
  • D. Strom MC (next)
  • Simulation by D. Freytag
  • Check with V. Radeka:
    “Effective shaping time is 40ns;
    so \(\sigma \approx 40/(S/N) \approx 5 \text{ ns or better}.”
Timing MC

Toy Monte Carlo Studies of Timing Resolution for 30 Samples

Assumptions – wild guesses – (waiting for real electronics model):

- Each MIP has 30 samples at random distances from the read-out chip
- Threshold for timing measurement is 8,000 electrons.
- Input FET has $g_m = 1.5\,\text{mS}$ and the noise contribution from the rest of the amplifier is equal to input FET except for the "floor" noise.
- The charge measurement has a noise floor of either 0 or 4000 electrons
- Time constant for charge measurement is 200 ns.
- Time constant for the time measurement is 50 or 200 ns.
- The noise signals in the timing and charge circuits are uncorrelated
- Random 5% channel to channel variation in threshold
- Random 1% event-to-event variation in threshold
- Random 5% uncertainty in constants used for correction.
- Reject time measurements far from mean
Timing MC (contd)

Sample Timing Results
200 ns time constant, no noise floor

Time versus charge for mips  30 sample average time

Entries  10000
Mean   -0.3855
RMS    2.194
Timing MC (contd)

50 ns time constant and 30-sample average

![Graph showing reconstructed time vs. number of events with mean and RMS values.]

Concerns & Issues:

- Needs testing with real electronics and detectors
- Verification in test beam
- Synchronization of clocks (1 part in 20)
- Physics crosstalk

- For now, assume pileup window is ~5 ns (3 bx)

Needs to be demonstrated in a test beam!
Power

- Use power cycling (short LC live times) to keep average power in check
- 40 mW and no Cu look to be realistic options

Bunch trains at 120 Hz
Bunch crossings at 1.4 ns

8.33 ms

270 ns
## Power (contd.)

<table>
<thead>
<tr>
<th>Phase</th>
<th>Current (mA)</th>
<th>Instantaneous Power (mW)</th>
<th>Time begin (us)</th>
<th>Time End (us)</th>
<th>Duty Factor</th>
<th>Average Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>All Analog &quot;on&quot;</td>
<td>370</td>
<td>930</td>
<td>0</td>
<td>9</td>
<td>0.00108</td>
<td>1.0</td>
</tr>
<tr>
<td>Hold &quot;on&quot;, charge amp off</td>
<td>85</td>
<td>210</td>
<td>9</td>
<td>100</td>
<td>0.01092</td>
<td>2.3</td>
</tr>
<tr>
<td>Analog power down</td>
<td>4</td>
<td>10</td>
<td>100</td>
<td>8333</td>
<td>0.988</td>
<td>9.9</td>
</tr>
<tr>
<td>LVDS Receiver, etc</td>
<td>3</td>
<td>0</td>
<td>8333</td>
<td></td>
<td>1</td>
<td>3.0</td>
</tr>
<tr>
<td>Decode/Program</td>
<td>10</td>
<td>1</td>
<td>100</td>
<td></td>
<td>0.01188</td>
<td>0.1</td>
</tr>
<tr>
<td>ADC</td>
<td>100</td>
<td>10</td>
<td>500</td>
<td></td>
<td>0.0588</td>
<td>5.9</td>
</tr>
<tr>
<td>Readout</td>
<td>50</td>
<td>500</td>
<td>2500</td>
<td></td>
<td>0.24001</td>
<td>12.0</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>459</strong></td>
<td><strong>1313</strong></td>
<td></td>
<td></td>
<td></td>
<td><strong>34.2</strong></td>
</tr>
</tbody>
</table>

- < 40 mW per wafer (∼10^3 pixels)
  - Passive cooling by conductance in W to module edges
    - $\Delta T \leq 5^\circ$ from center to edge
  - Maintains small gap & Moliere radius

Cooling

**ECAL**
• Even though accelerator live fractions are $3 \times 10^{-5}$ (warm) and $5 \times 10^{-3}$ (cold), current electronics design parameters give small difference
• Shouldn’t need copper heat sink if present heat load estimates are correct (or close to correct).
  Angle = 11 mrad
• Compare with effective Moliere radius of 3mm at 1.7m (CALICE?):
  Angle = 13 mrad
• Capacitors may be biggest challenge
Components in hand

**Tungsten**
- Rolled 2.5mm
  - 1mm still OK
- Very good quality
  - < 30 µm variations
- 92.5% W alloy
- Pieces up to 1m long possible

**Silicon**
- Hamamatsu detectors
- Should have first lab measurements soon
- (Practicing on old 1cm dets.)