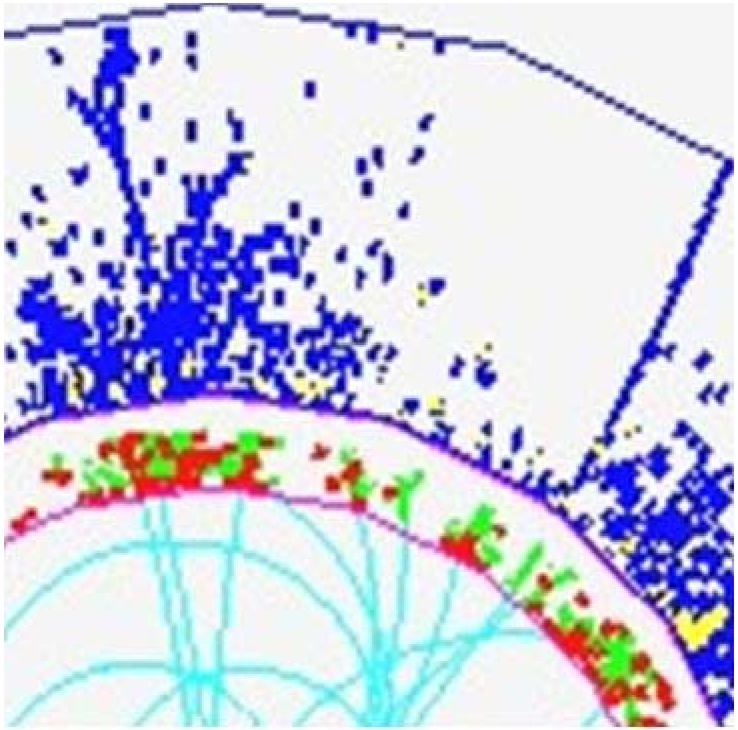
a few selected calorimeter-related
items from Paris LCWS

Ray Frey

LCD May 20, 2004



Items of special interest (to me) …

- warm vs cold
  - backgrounds
    - Tim (2 weeks ago)
    - K. Desch
  - timing
  - forward cal (last week)
- revisiting global detector design
- particle flow
- Si/W ECal

Warm or Cold ??

Implications on detector design

(my opinion: small effects)

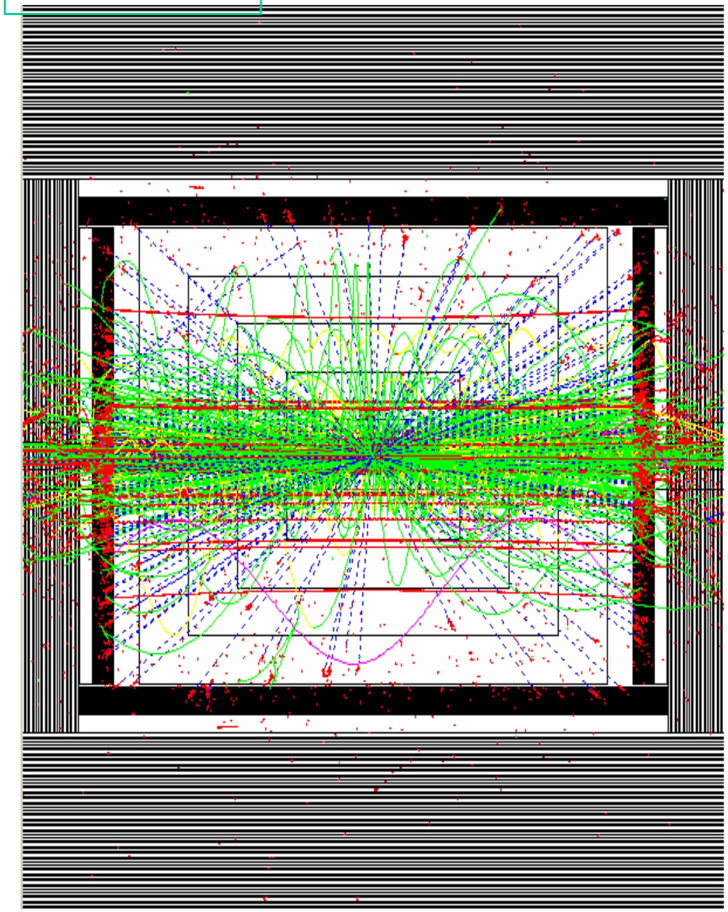
- energy spread
- bunch timing structure
- crossing angle

Timing is good

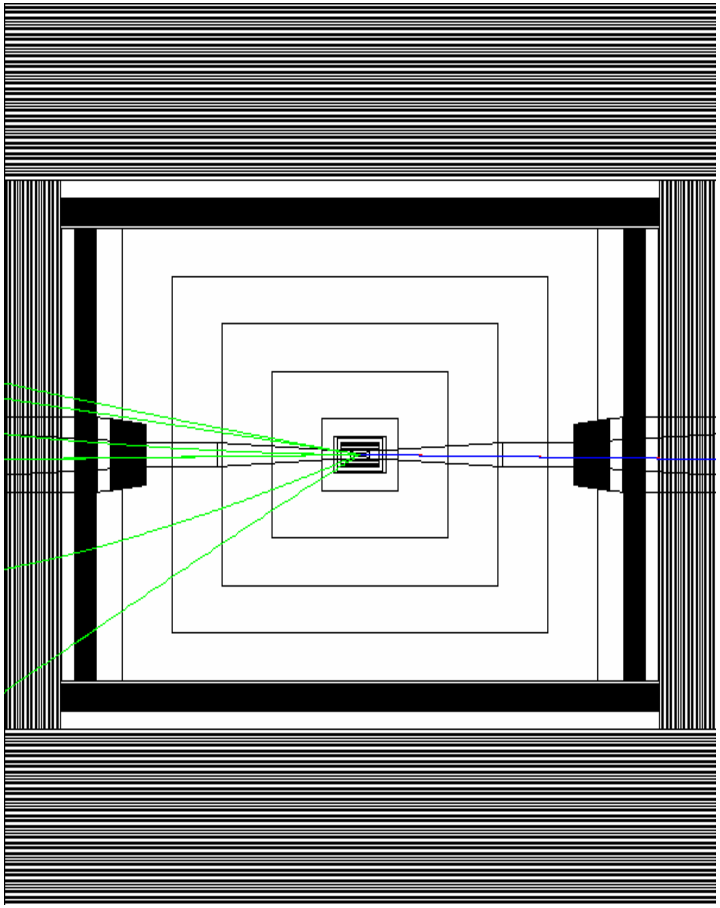
Warm detector concern:

Pileup of $\gamma\gamma \rightarrow$ hadrons over bx train

T. Barklow



Si/W ECal
Timing ~ 1 ns



192 bx pileup
(56 Hadronic Events/Train)

3 bx pileup (5ns)

Timing and Bunch Structure

- Warm-Cold Differences and Possible Implications
- Background Characteristics
- Hadronic Background: Impact on Physics

Klaus Desch, University of Hamburg

LCWS04, Paris, 20/04/04

What can be achieved?

Tracking:

Studies indicate 2-5 ns track timing possible in principle for TPC and Si
Detailed time-dependent simulation needed – non-trivial

Calorimetry (most important in central detector, many neutrals):

With electronics inside Si-W calorimeter 5ns for single cells achievable in SLAC design
Averaging over 30 hits: 5 ns / sqrt(30) = 1 ns (Jaros, Frey)

Concerns:

- Distribute o(GHz) clock over a large detector
- Timing calibration for o(10^8) cells (o(10^5) r/o chips) to ns precision
- Cluster finding to do the averaging – need detailed time-dependent simulation
- Charged particles in endcap: time-of-flight correction (loopers!)

Preliminary Summary

Integrating the hadronic background from more than a few bunch-crossings has a sizeable impact on the physics performance

America, Asian, and European studies agree

At NLC, a bunch tagging of few ns is needed to become comparable to the TESLA situation

→ R&D on detector timing is vital for warm technology

→ Timing capability adds complexity – how much?

Revisiting global detector design

- Special parallel session on global design
- Brient:
  - Reconsidering TESLA TDR detector
  - Merging SiD and TDR

- Keeping the current R&D consortia (eg CALICE)

- Two leading detector models: TDR and SiD
- How to “internationalize” the involvements

Two detector options today .... SD vs TDR [*]

TRACKER	SD	TDR
	Silicon tracker	TPC and Si envelope
CALORIMETRY		
ECAL	tungsten-silicon both options	
HCAL	Digital (RPC,GEM,..)	Digital / Tile AHCAL

Partly the same people

[*] J.Jaros at ALCPG-SLAC04

The 2 options following J.Jaros

Silicon area TDR / Silicon area SiD ~ 2.6

The only(main) justification for the SD detector ??!!

	TESLA	SD	LD	JLC
Tracker type	TPC	Silicon	TPC	Jet-cell drift
ECAL				
R_{min} barrel (m)	1.68	1.27	2.00	1.60
Type	Si pad/W	Si pad/W	scint. tile/Pb	scint. tile/Pb
Sampling	$30 \times 0.4X_0$ $+10 \times 1.2X_0$	$30 \times 0.71X_0$	$40 \times 0.71X_0$	[illegible] $\times 0.71X_0$ 2
Gaps (active) (mm)	2.5 (0.5 Si)	2.5 (0.3 Si)	1 (scint.)	1 (scint.)
Long. readouts	40	30	10	3
Trans. seg. (cm)	≈ 1	0.5	5.2	144
Channels ($\times 10^3$)	32000	50000	135	5
Z_{min} endcap (m)	2.8	1.7	3.0	1.9
HCAL				
R_{min} (m) barrel	1.91	1.43	2.50	2.0
Type	T: scint. tile/S.Steel D: digital/S.Steel	digital	scint. tile/Pb	scint. tile/Pb
Sampling	$38 \times 0.12\lambda$ (B), $53 \times 0.12\lambda$ (EC)	$34 \times 0.12\lambda$	$120 \times 0.047\lambda$	1[illegible] $\times 0.047\lambda$ 3
Gaps (active) (mm)	T: 6.5 (5 scint.) D: 6.5 (TBD)	1 (TBD)	2 (scint.)	2 (scint.)
Longitudinal readouts	T: 9(B), 12(EC) D: 38(B), 53(EC)	34	3	4
Transverse segmentation (cm)	T: 5–25 D: 1	1	19	14
θ_{min} endcap	5°	2°	2°	8°
Coil				
R_{min} (m)	3.0	2.5	3.7	3.7
B (T)	4	5	3	3
			option: Si pad shower max. det.	scint. strip (1 cm) shower max. det. (2 layers)

TDR geometry

Radius, length, size, ...

Tracker size

Reason for 2.50m for the TPC length
- Covering at low angle ? but the FTD is doing it with FCH

Reason for the TPC radius of 1.60m
- Single track resolution ?
- Separability ?

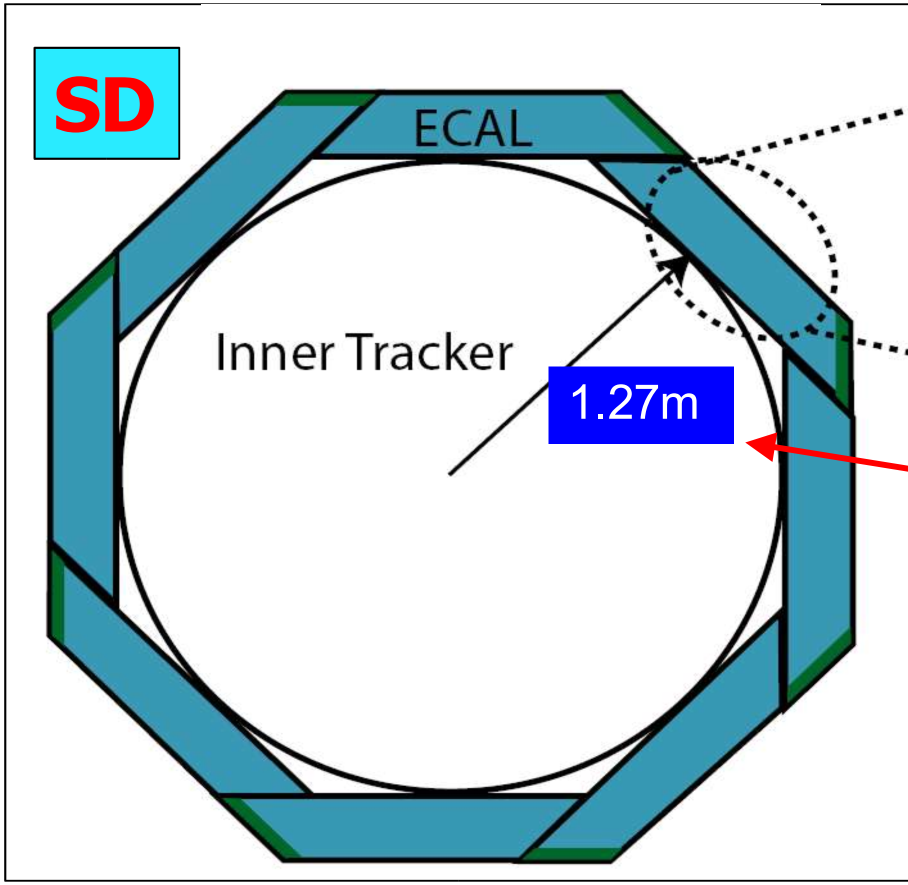
ECAL size

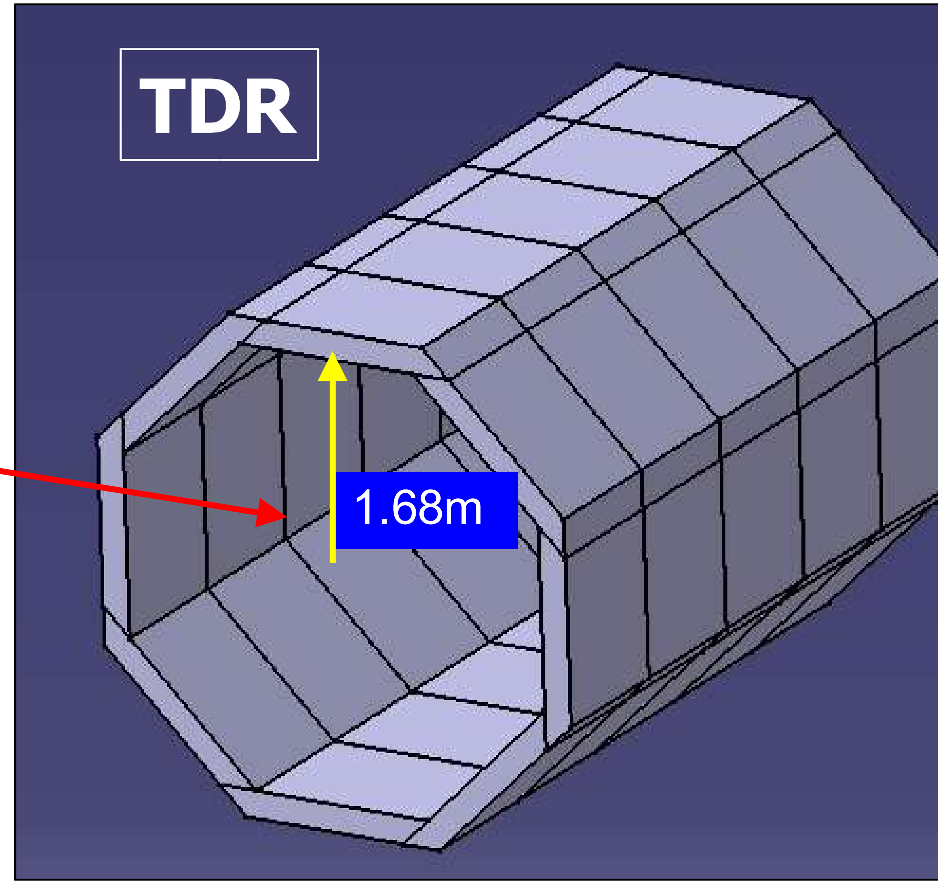
Reason for 1.70m for the ECAL radius
- TPC radius + 10cm
- Compact ECAL to save space for HCAL inside coil

Reducing the external radius of the TPC (reduce the cost of the overall detector)
- Impact on the momentum resolution ?
- if needed a precise point outside TPC can be added ??
- what about the charged-neutral separation ??

Geometry of the calorimeter

ECAL-SiD- ALCPG ⟷ ECAL-TDR- CALICE





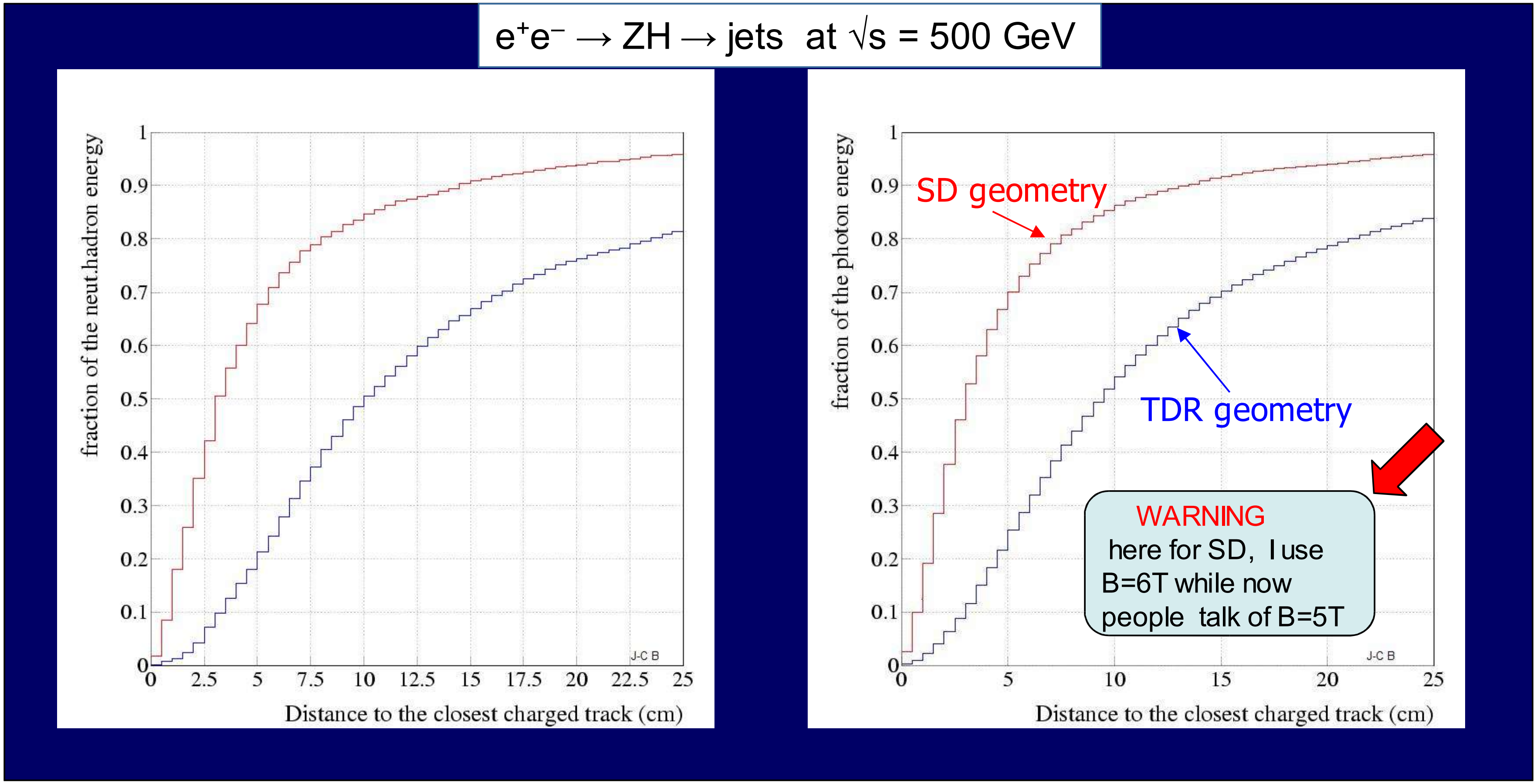
Is it so different ?

At least , there is a good agreement on the global geometry

The ECAL internal radius

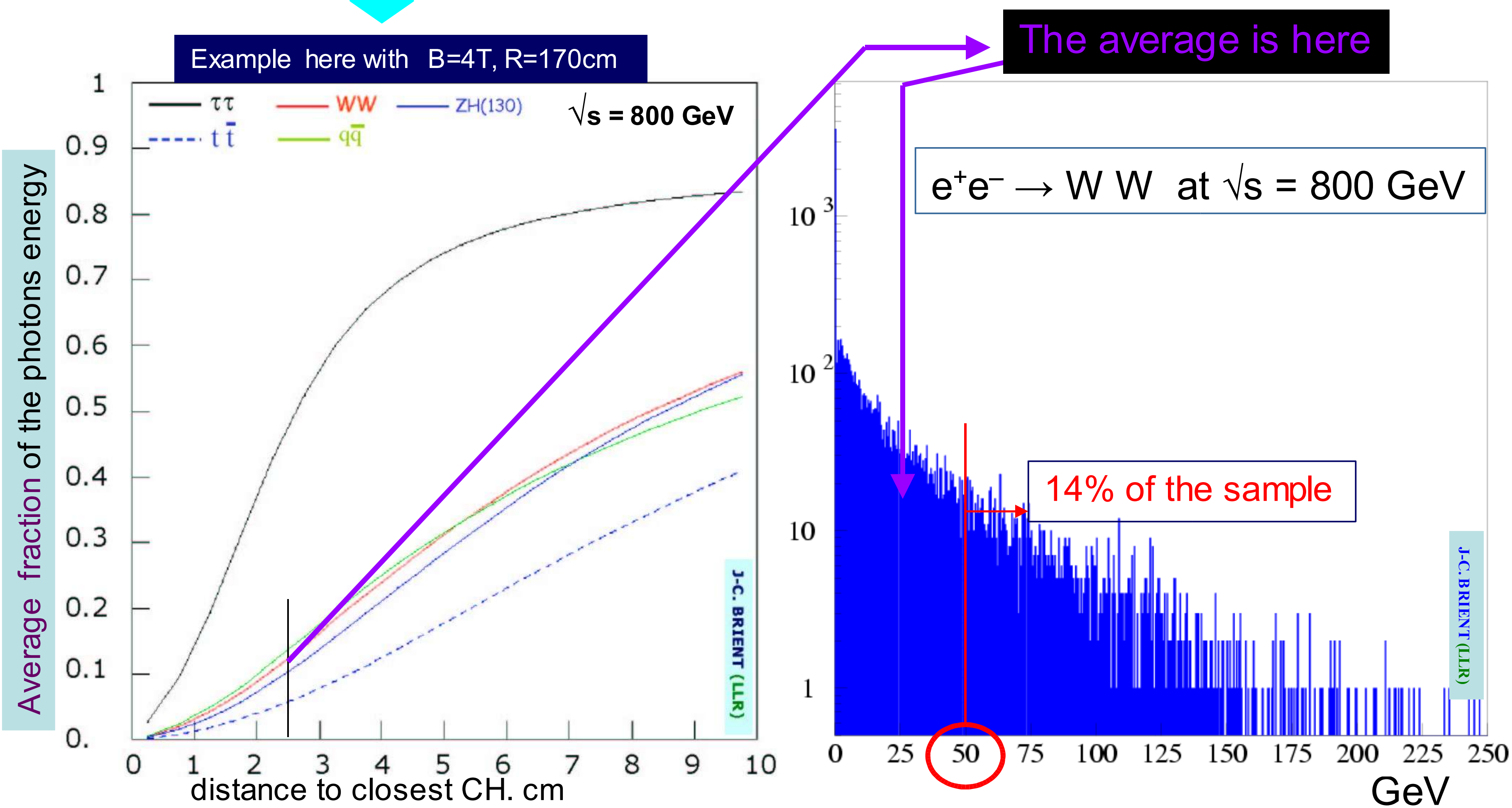
Impact on EFLOW

Presentation JCB at LBL 2000 – ALC meeting



For SD geometry, there is an average of **~65GeV** of photons closer than 2.5 cm versus **~20 GeV** for the TDR geometry

What for different physics process



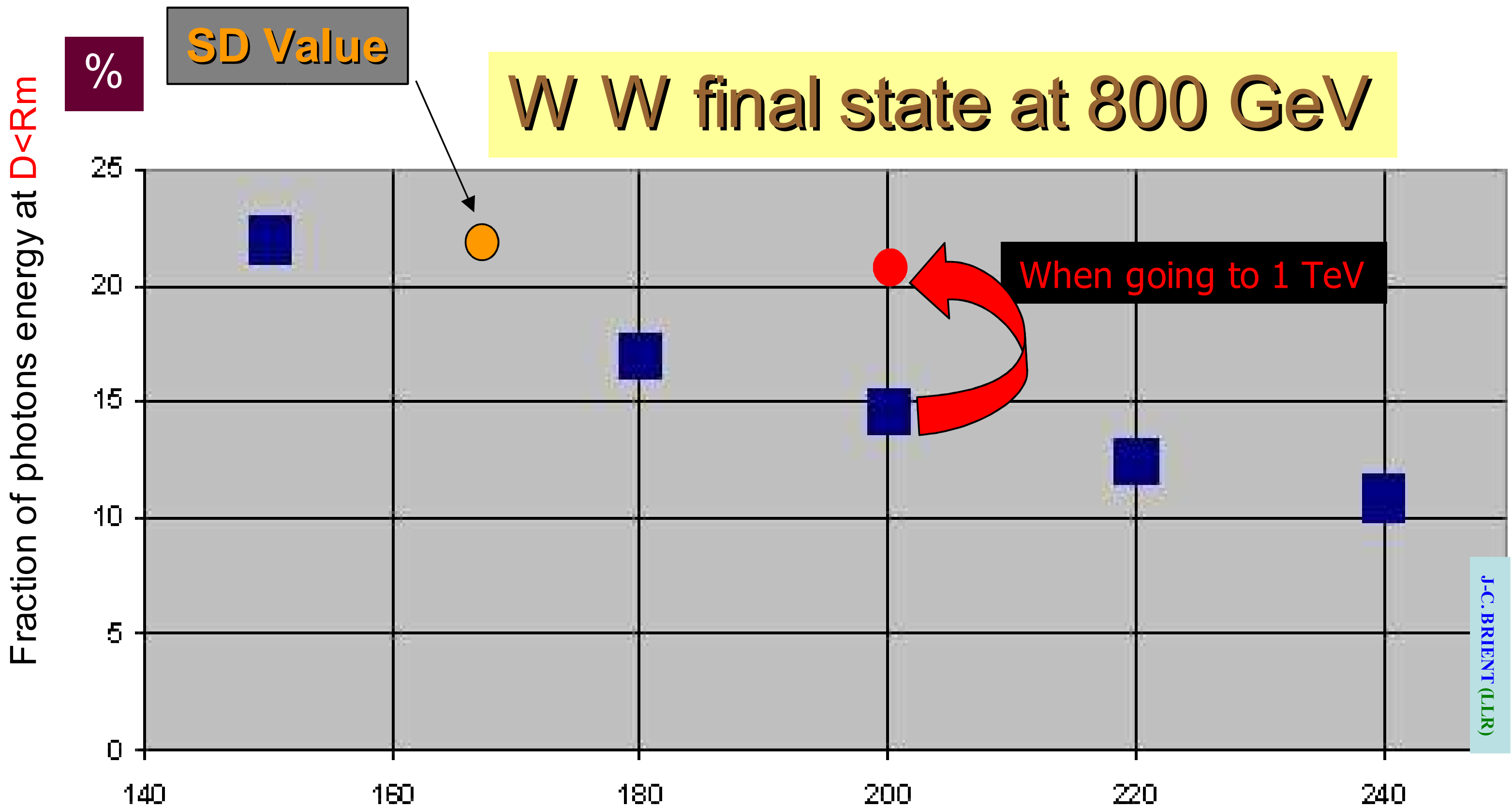
Efficiency of reconstructing photons close to ch. track (D<Rm) is **<<100%**

Variation with the ECAL endcap entrance

Internal radius fixed at 1.50 m and B=4T

Length of the TPC

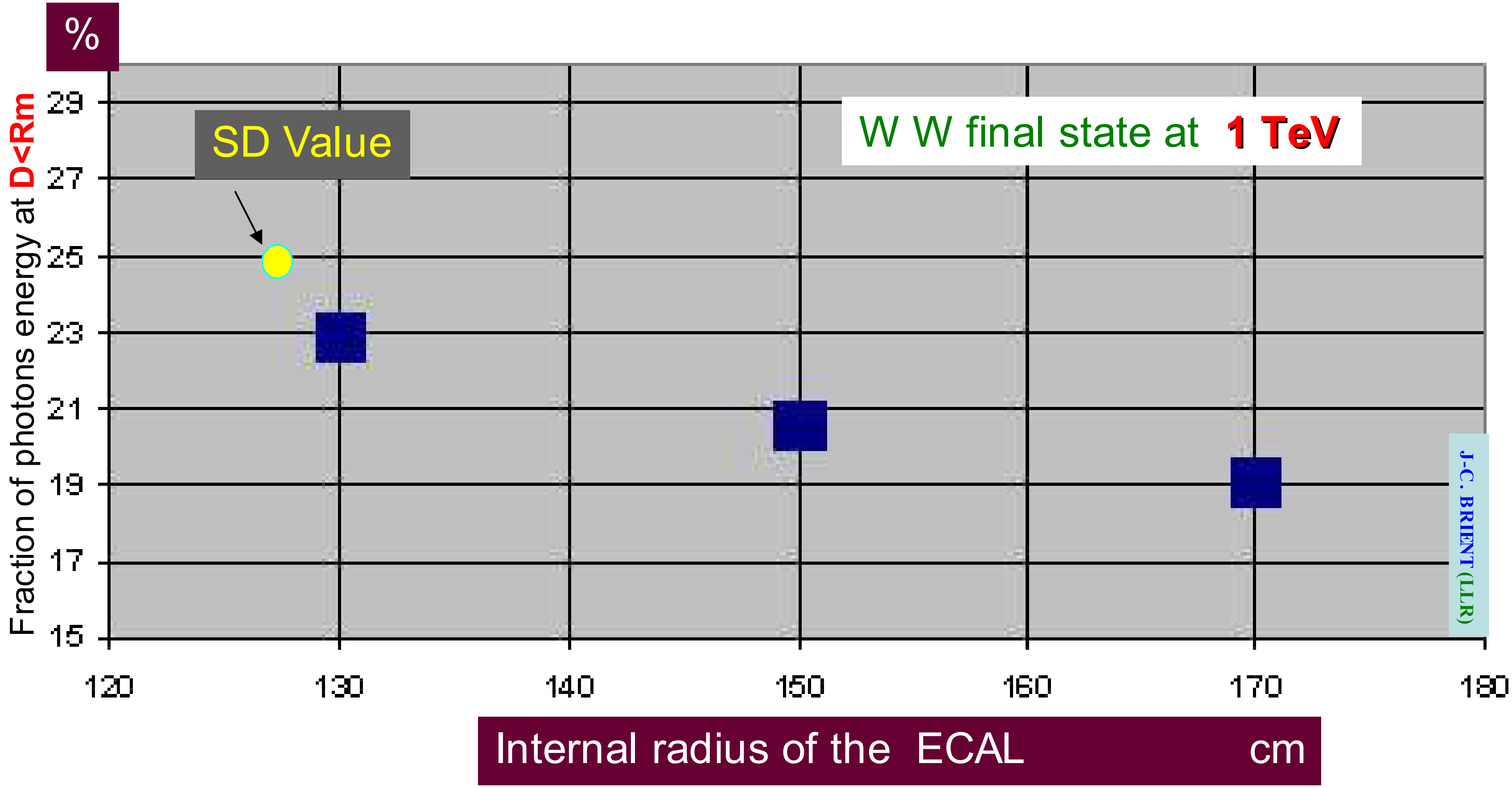
We define Rm at 2cm



Distance of the ECAL endcap

Variation with the internal ECAL radius

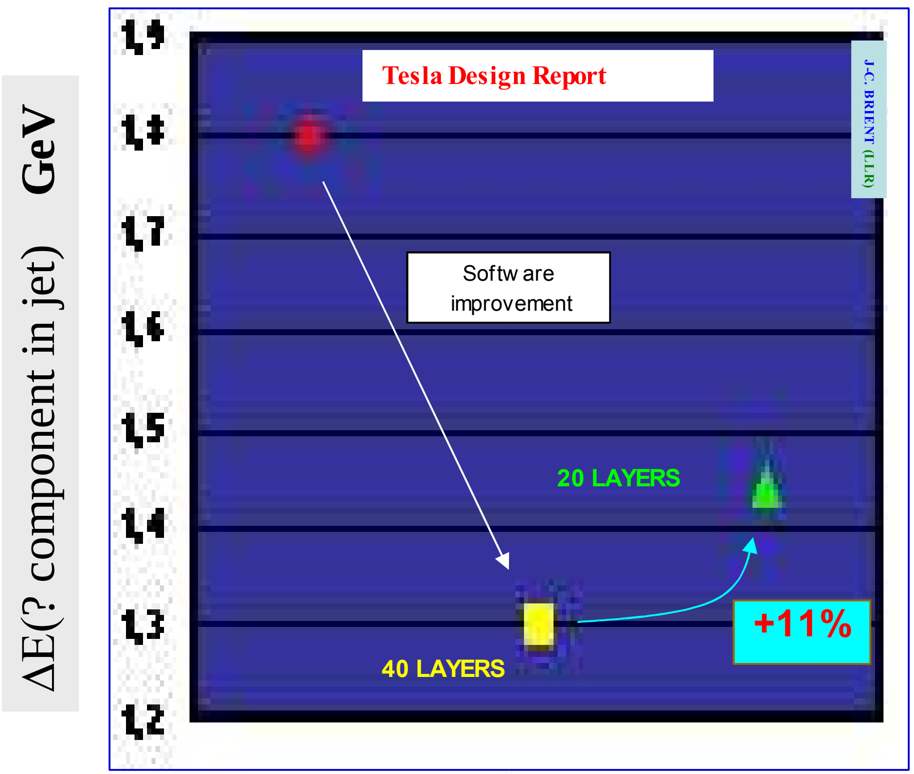
Z endcap at 2.00 m and B=4T



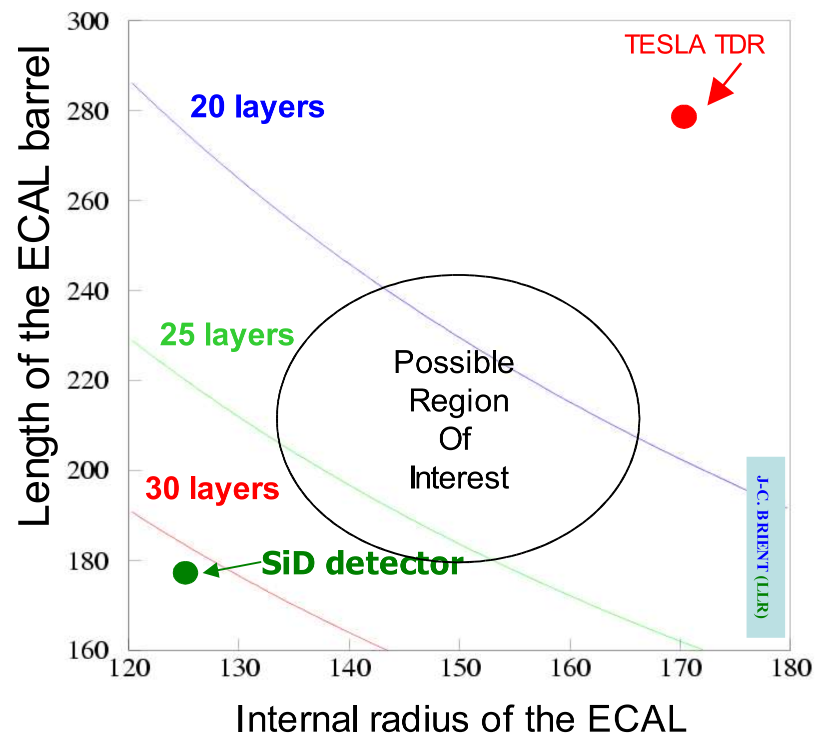
SD Values Rint=125, Zec=170 and B=5T

Is it possible reducing the calor. cost ? AND saving the EFLOW performances

ECFA Krakow Sept. 2001



Curves ISOCOST(area) versus SiD



W W at 800 GeV

The relevant law is in BR^2/Rm

VERY IMPORTANT NUMBERS

For the TDR type of detector (R=170cm and 4T)
14% of the events have more than 50 GeV in the difficult region

For the SiD detector (R=125cm and 5T)
32% of the events have more than 50 GeV in the difficult region

Due to the large value of the WW cross section,
Any signal in jets could be overflowed ?!

For the photon(s) reconstruction , the ECAL radius and Z endcap is much more important !!!
Impact on the jets to be quantified ?

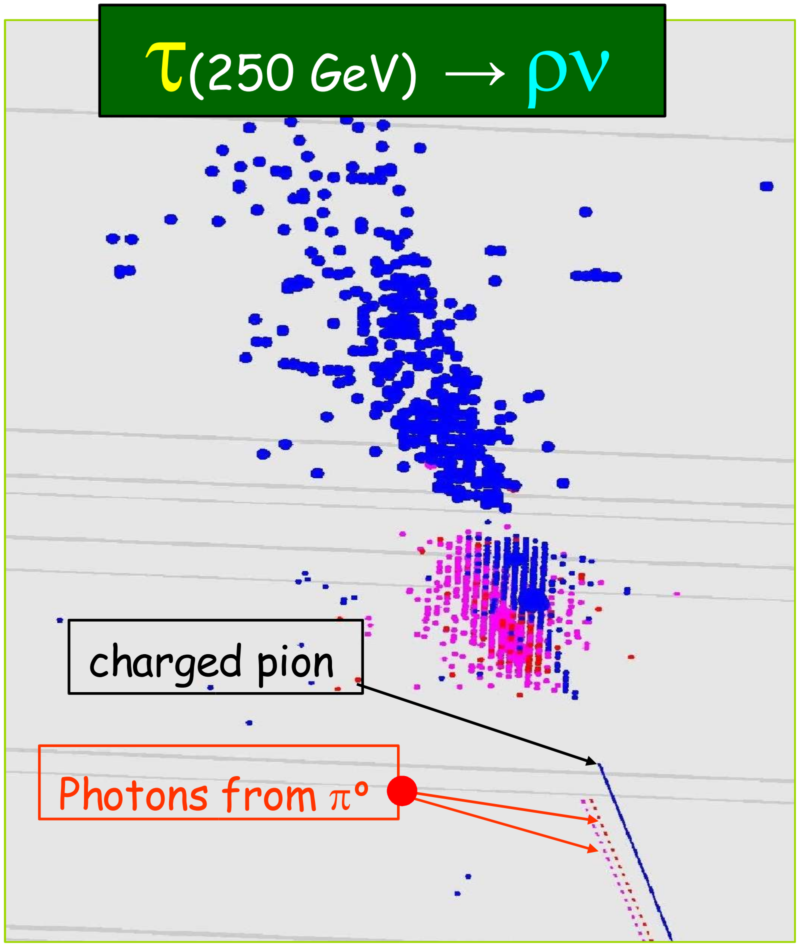
To reduce the ECAL cost,
Playing with layers number is more efficient and less penalizing for the performances on jet , τ ,... ?!

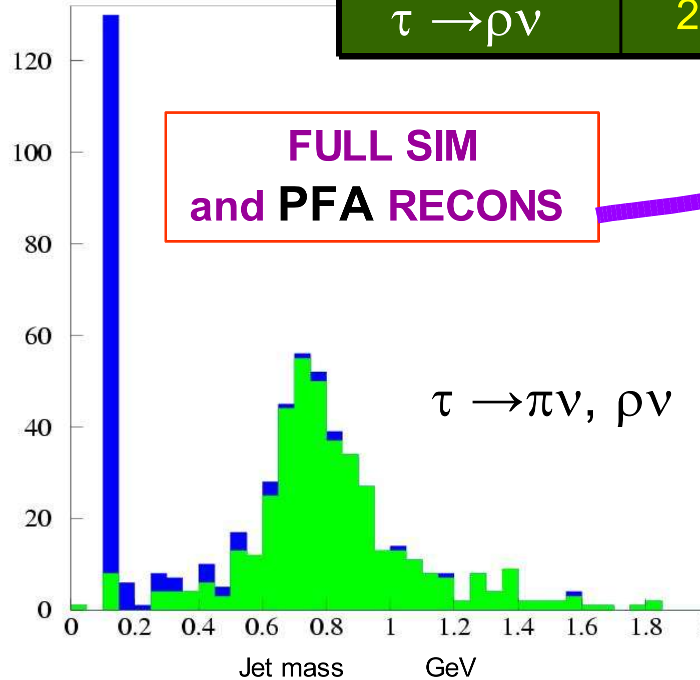
A new detector proposal

~ 20-25 layers ECAL at R≈1.55m ?? Z_{ECAL} ??

Tau decays ID is essential for τ ID and polarisation measurement

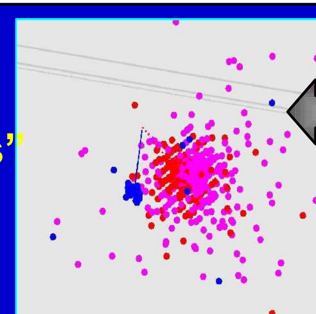
	Jet mass < 0.2	Jet mass in 0.2-2
$\tau \rightarrow \pi\nu$	82%	17%
$\tau \rightarrow \rho\nu$	2%	90%



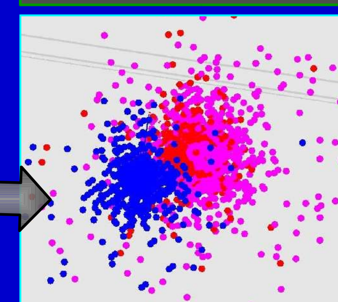


FULL SIM and PFA RECONS

Why "continuous" readout is needed



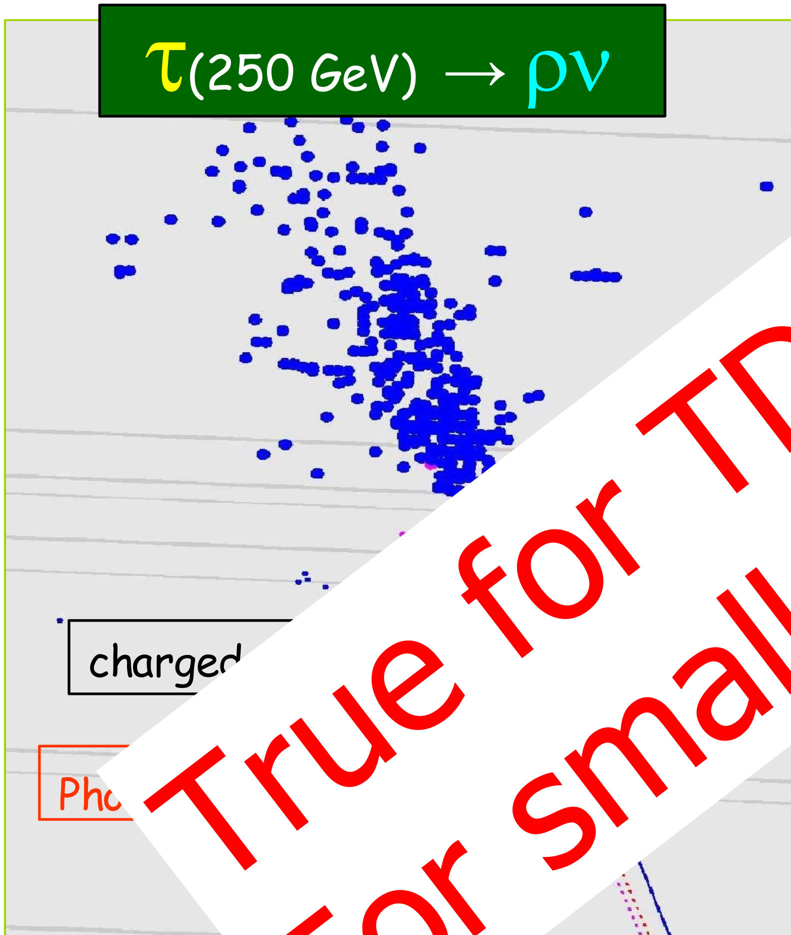
Looking along the charged track in the first 4 X0

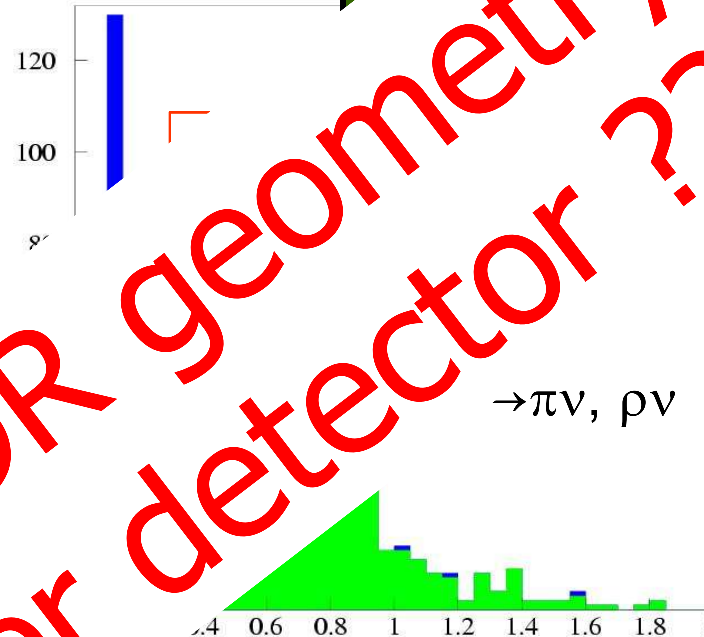


Looking along the charged track in 5-12 X0

Tau decays ID is essential for τ ID and polarisation measurement

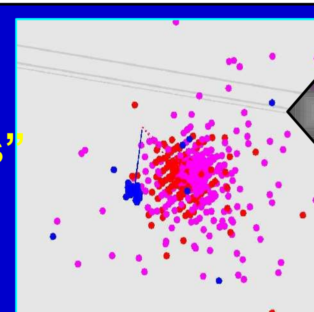
	…t mass …0.2	Jet mass in 0.2-2
τ …	…%	17%
		90%



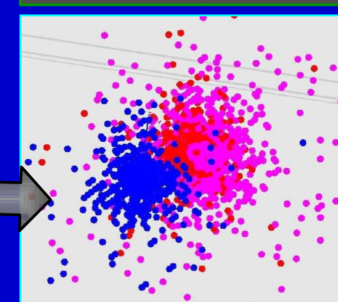


True for TDR geometry
For smaller detector ??

Why "continuous" readout is needed



Looking along the charged track in the first 4 X0



Looking along the charged track in 5-12 X0

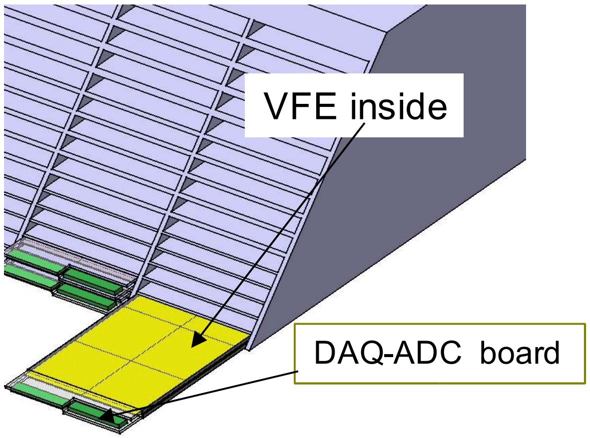
Summary of the ECAL change vs TDR

- ► VFE inside for the ECAL, alveoli thinner , better eff. Molière radius
- ► For the simulation, I propose to use 30 layers to be consistent with the SiD ECAL and with the prototype in construction

Changing the general geometry

- ► VFE inside for the HCAL (Si-PM, or digital readout for DHCAL)
  - → NO SPACE for fibbers in overlap !!! ☺
  - → NEW distance TPC-ECAL in endcap !!!!

New way of the ECAL readout



VFE (with ADC?) send each BX to DAQ board (with/without ADC)
DAQ-ADC board digitise, store in digital memory, MUX to optical link

- VFE time occupancy is about 1/200 for TESLA
- VFE On-Off take about 100 μs

⇒ Simulation gives **~100μW**/channel !!! (source CdIT)

Passive cooling would be sufficient (source JB)

R&D in CALICE ECAL **(IN2P3,KNU,MSU)**
to quantify this **passive cooling limit**

Modify Simulation
(better R_m^{eff})

Other open questions

- Quantitative variation of performances on jet(s)
  (and impact on physics program) with TPC size

- Is there a way to avoid the hole between Forward CAL and ECAL together with the possibility to open the detector ?

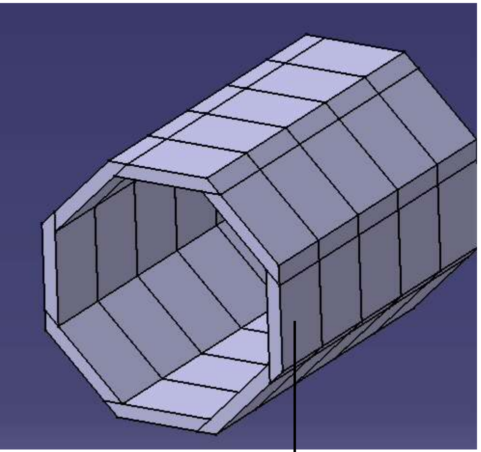
- A dedicated study of the CALOR. endcap geometry

- Using ECAL to seed the high Pt track in the SiD tracker ?
  a kind of substitute for the large number of points in a TPC

- FCH (SET?) in silicon device inserted in ECAL CFi frame ? **See next slide**

- What is the **number of X0** of the endplate and readout electronics ?
  what is the distance TPC-ECAL ?

If precise point(s) outside TPC is mandatory

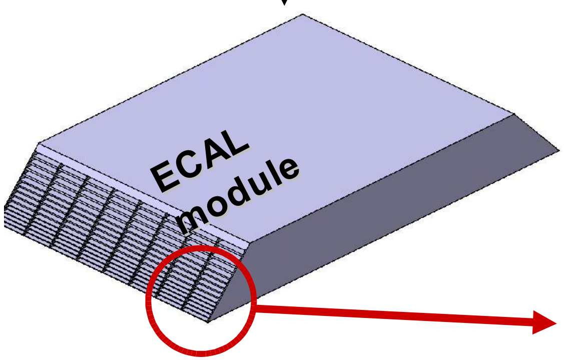


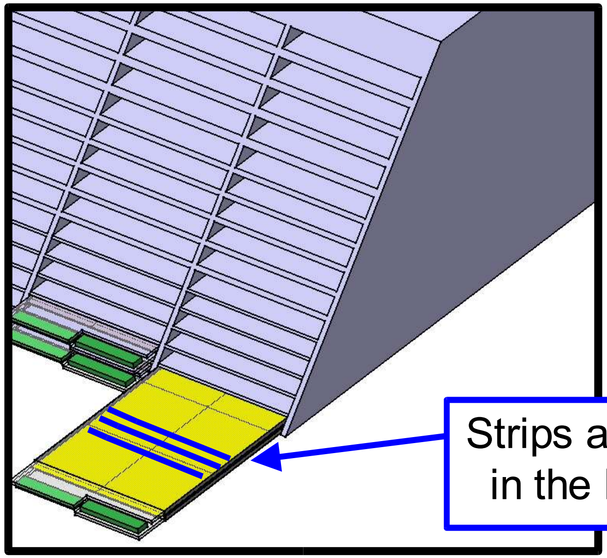
Add alveoli with 2 double side strips without tungsten

- Minimize the thickness/"tracker point"
- Minimize the distance to the ECAL
- Minimize the inter alignment tracker-ECAL

and

ASSEMBLING SIMPLICITY





Strips along RΦ in the barrel

ΔZ ≤ Strip Width

A lot of questions , Just few answers/guess

I propose you my preliminary ***personal conclusions***

- For CALOR. geometry , the TDR detector is not so different from the SD detector, but the size
- The PFLOW is **very** probably more difficult with the SD detector (to be quantified)
- The impact on the performances from different TPC size, with/without precise points, etc… has to be QUANTIFY

May be it is time to begin the second round of detector optimisation

- Inter-regional proposal would be **VERY WELCOME** !!
- a proposal at the next LCWS ?

Where to go?

- SiD has the lead for the implementation of SiW as an ECal technology (blatantly biased personal opinion)
- But ignoring cost, the reduced radius of SiD is a disadvantage for performance

- TDR and SiD: save money by reducing the number of layers
  - Need to quantify the performance costs
- For TDR: reduce cost by reducing radius
- For SiD: increase performance by increasing radius

- Does it make sense to work toward a common global concept ?
- Decouple this from technological implementation, which can remain on separate paths ?

SD Si/W

M. Breidenbach, D. Freytag, N. Graf, G. Haller, O. Milgrome

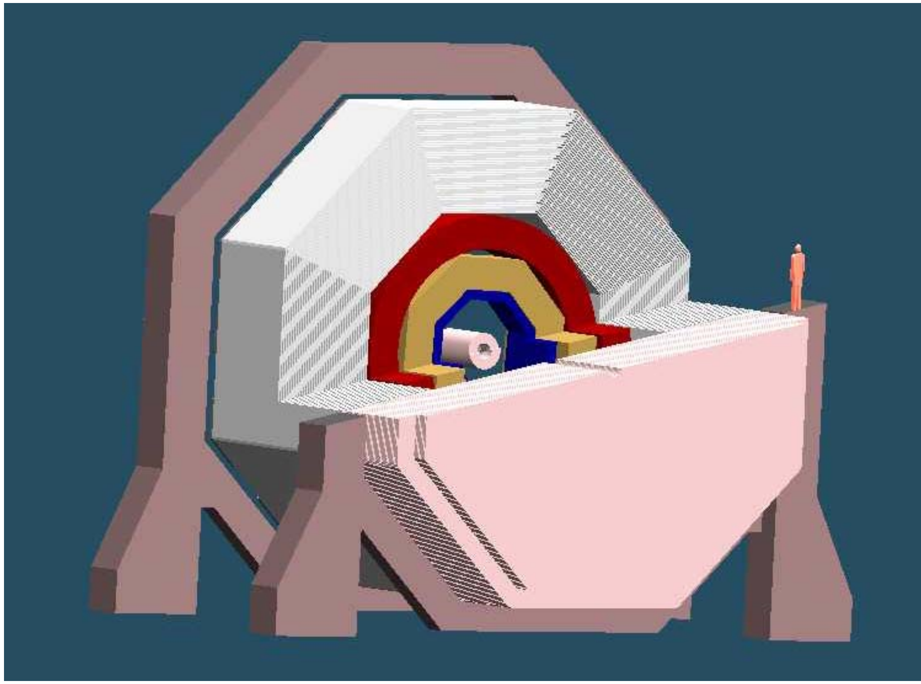
Stanford Linear Accelerator Center

R. Frey, D. Strom

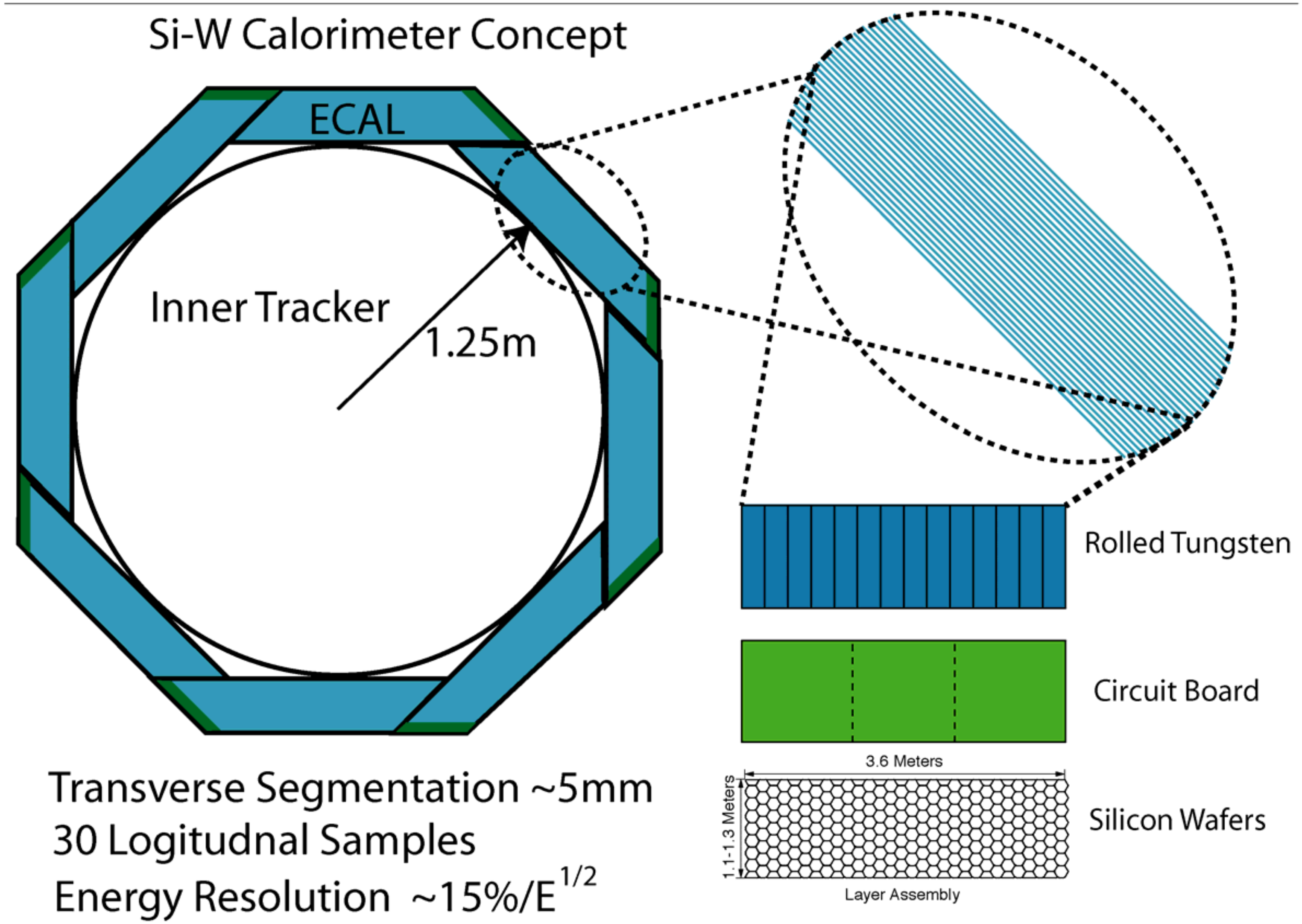
U. Oregon

V. Radeka

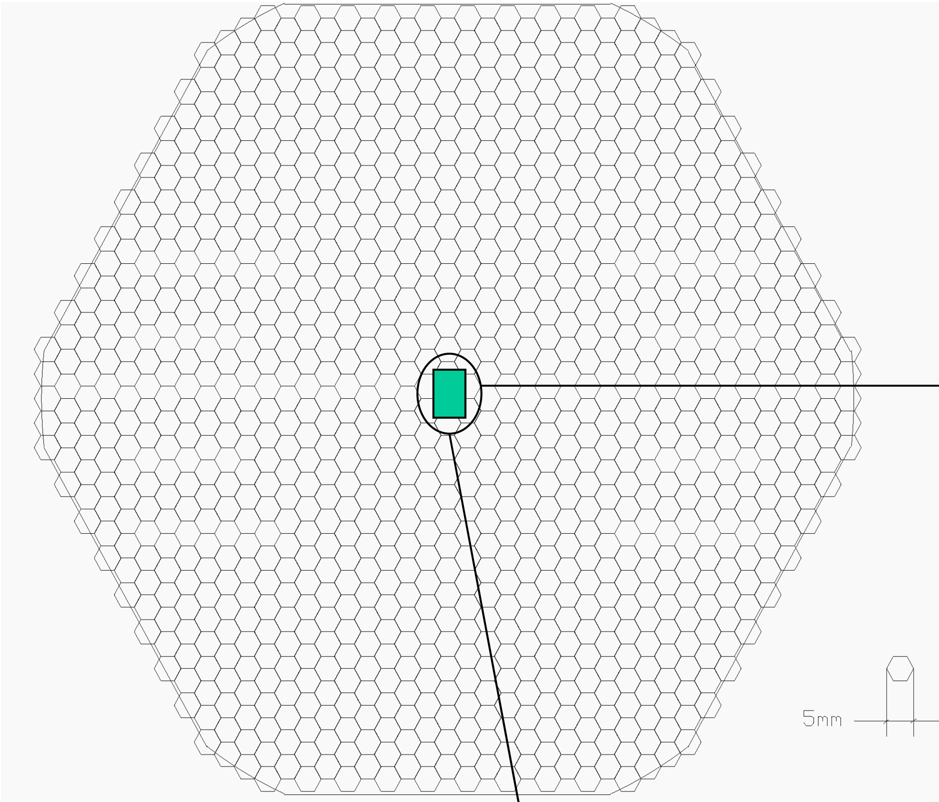
Brookhaven National Lab

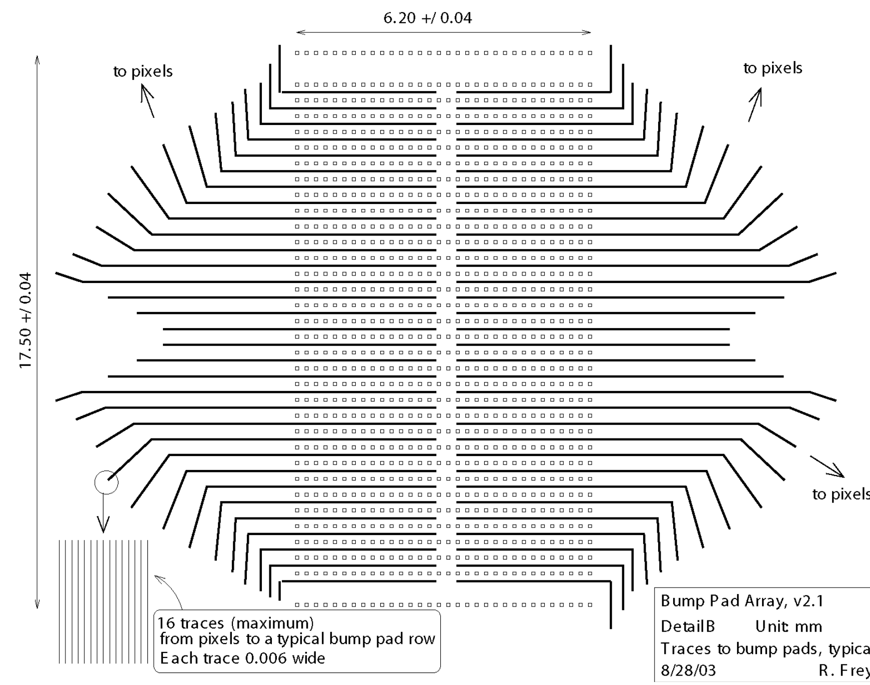


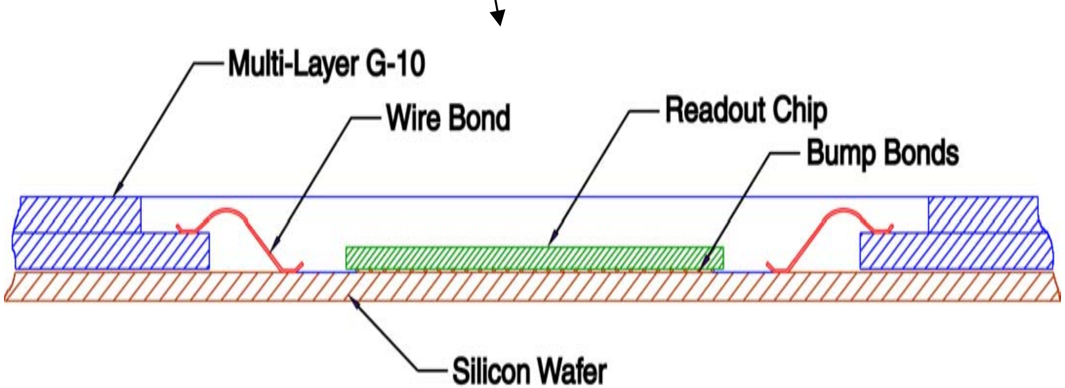
Concept

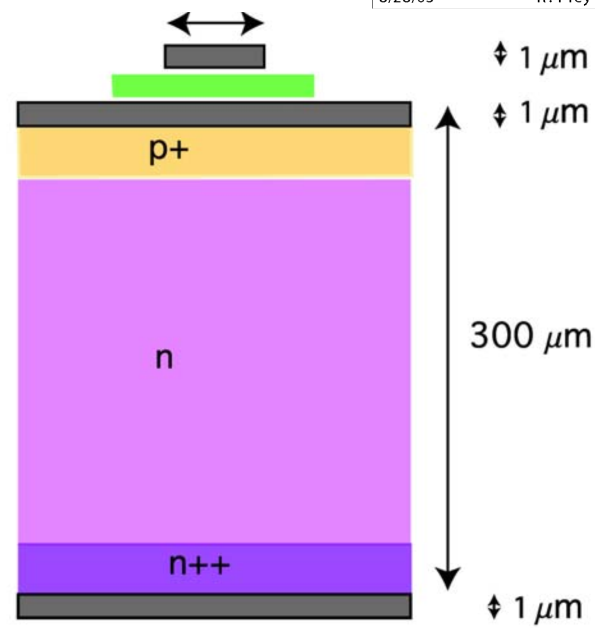

Si-W Calorimeter Concept
ECAL
Inner Tracker
1.25m
Rolled Tungsten
Circuit Board
3.6 Meters
1.1-1.3 Meters
Silicon Wafers
Layer Assembly
Transverse Segmentation ~5mm
30 Logitudnal Samples
Energy Resolution ~15%/E^1/2

Wafer and readout chip





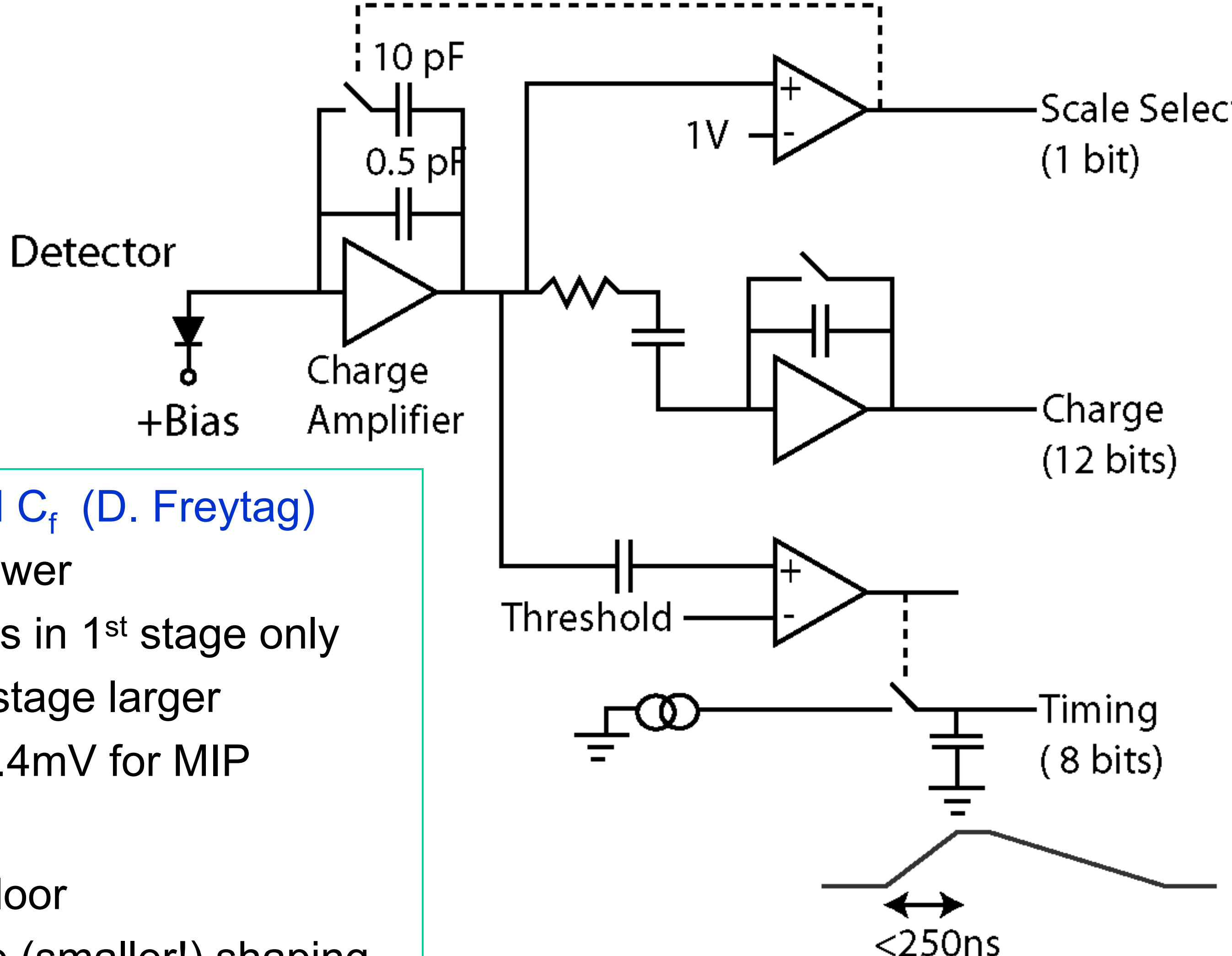




Electronics design – Present

Single-channel block diagram

Note: Common ~50 MHz clock



- Dynamically switched C_f (D. Freytag)
  - Much reduced power
    - Large currents in 1st stage only
  - Signals after 1st stage larger
    - ~0.1 mV → 6.4mV for MIP
- Time
  - No 4000e noise floor
  - Can use separate (smaller!) shaping time (~40 ns)
  - Readout zero-crossing discharge (time expansion)

Electronics design (contd)

- Present design gives:

  Noise = 20-30 e/pF
- C_{in} = pixel + traces + amplifier

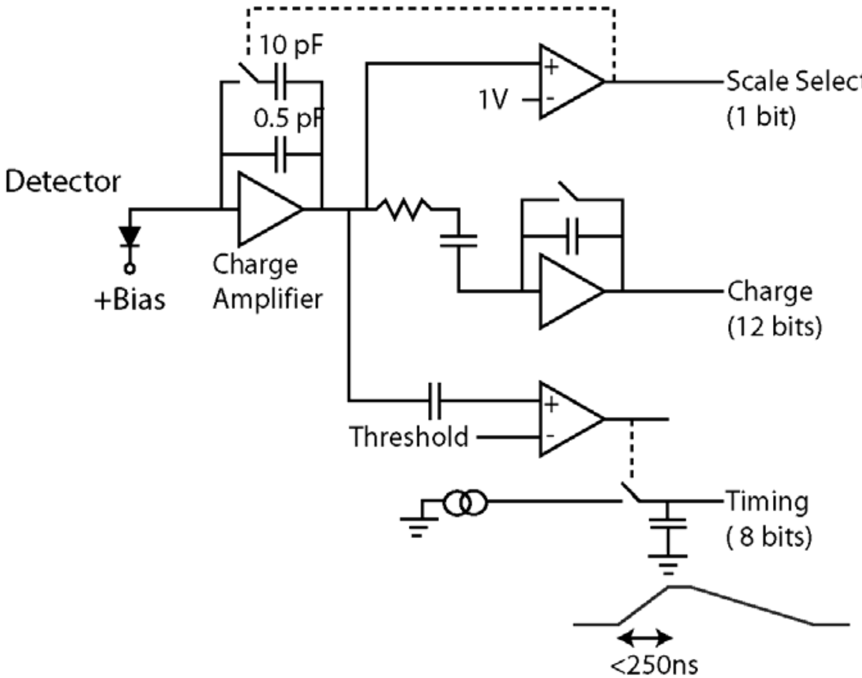
  5.7pF + 12pF + 10pF ≈ 30 pF

⇒ Noise ≈ 1000 e (MIP is 24000 e)

- Timing: ~ 5 ns per MIP per hit
  - D. Strom MC (next)
  - Simulation by D. Freytag
  - Check with V. Radeka:

    "Effective shaping time is 40ns;

    so σ ≈ 40/(S/N) ≈ 5 ns or better."



Timing MC

D. Strom, Calor2004

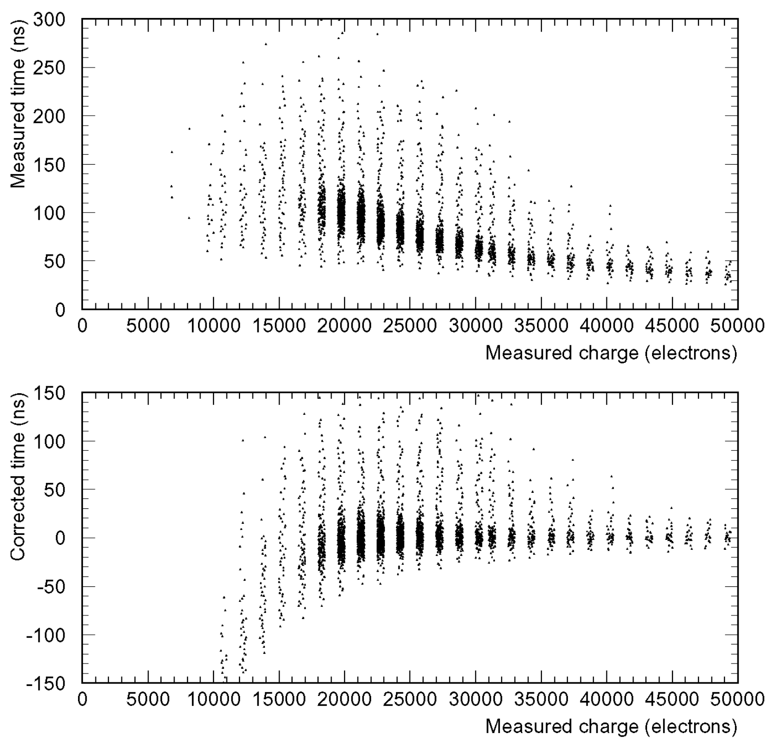
Toy Monte Carlo Studies of Timing Resolution for 30 Samples

Assumptions – wild guesses – (waiting for real electronics model):

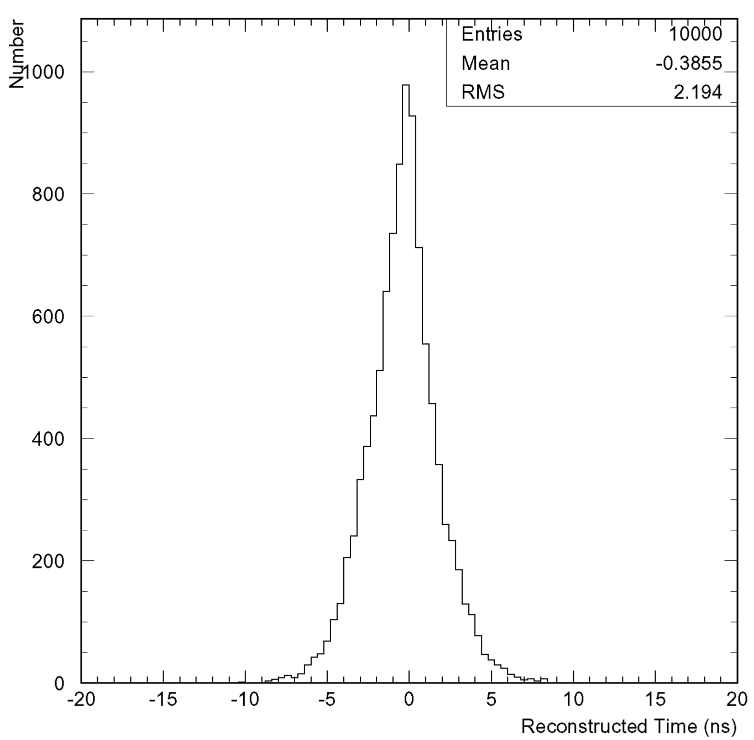
- Each MIP has 30 samples at random distances from the read-out chip
- Threshold for timing measurement is 8,000 electrons.
- Input FET has $g_m = 1.5$mS and the noise contribution from the rest of the amplifier is equal to input FET except for the "floor" noise.
- The charge measurement has a noise floor of either 0 or 4000 electrons
- Time constant for charge measurement is 200 ns.
- Time constant for the time measurement is 50 or 200 ns.
- The noise signals in the timing and charge circuits are uncorrelated
- Random 5% channel to channel variation in threshold
- Random 1% event-to-event variation in threshold
- Random 5% uncertainty in constants used for correction.
- Reject time measurements far from mean

Sample Timing Results

200 ns time constant, no noise floor



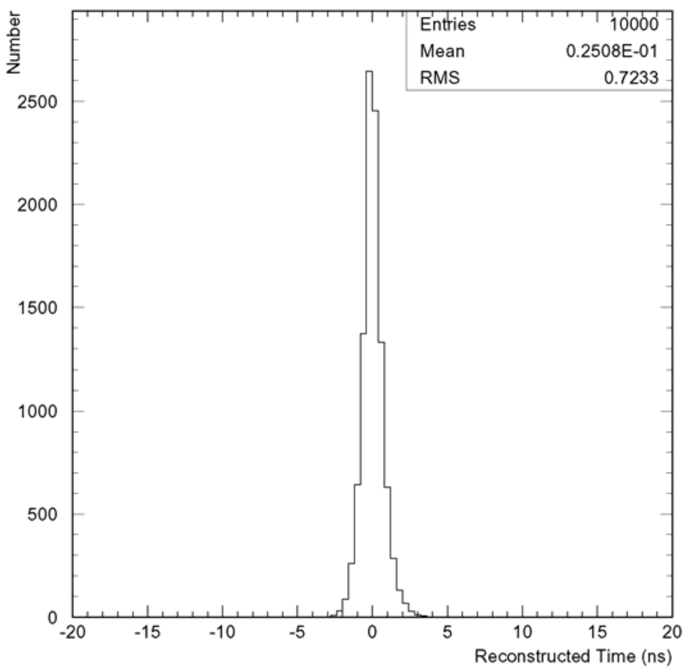
Time versus charge for mips



30 sample average time

Timing MC (contd)

50 ns time constant and
30-sample average



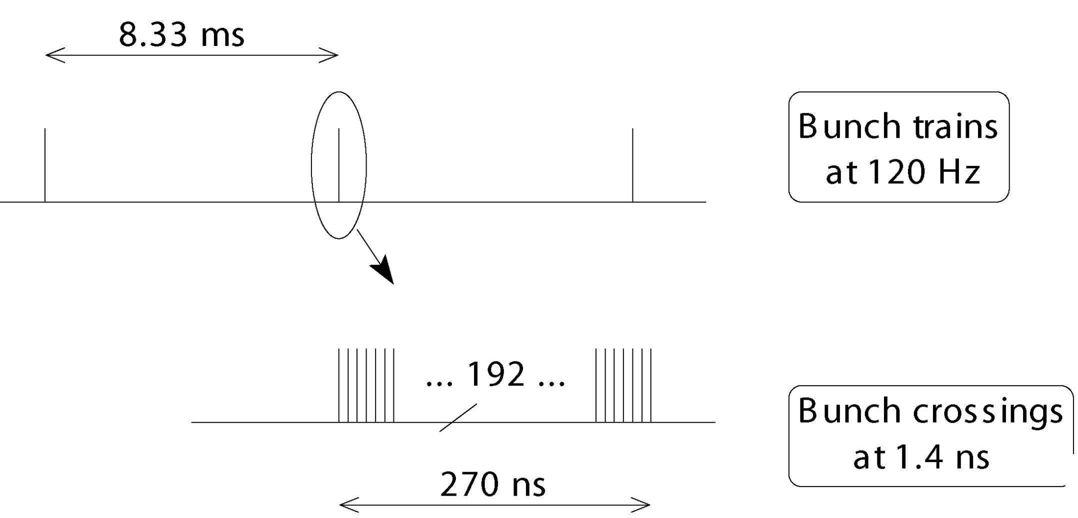
Needs to be demonstrated in a test beam!

Concerns & Issues:

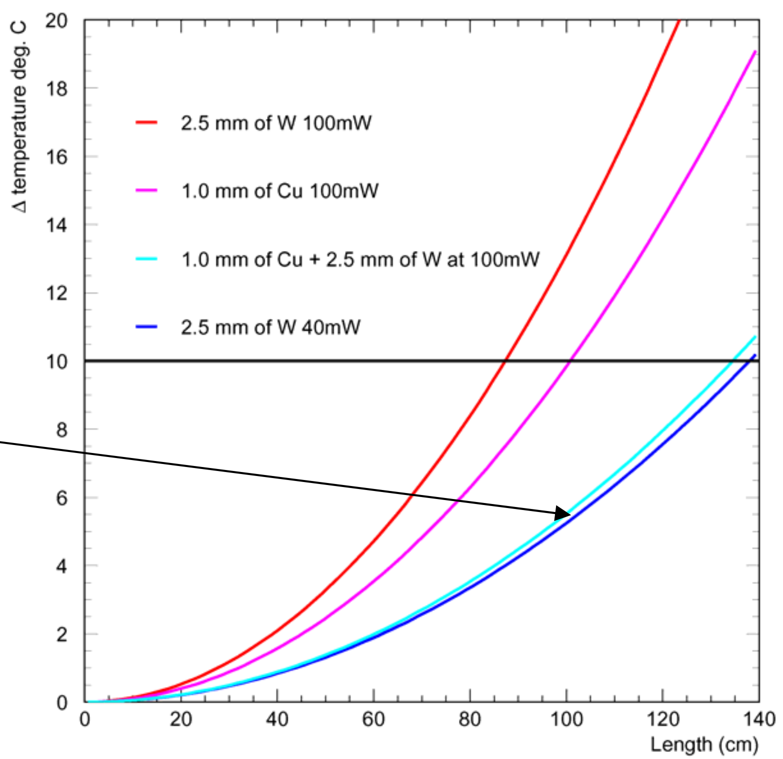
- Needs testing with real electronics and detectors
- verification in test beam
- synchronization of clocks (1 part in 20)
- physics crosstalk

- For now, assume pileup window is ~5 ns (3 bx)

Power



- Use power cycling (short LC live times) to keep average power in check
- 40 mW and no Cu look to be realistic options



Power (contd.)

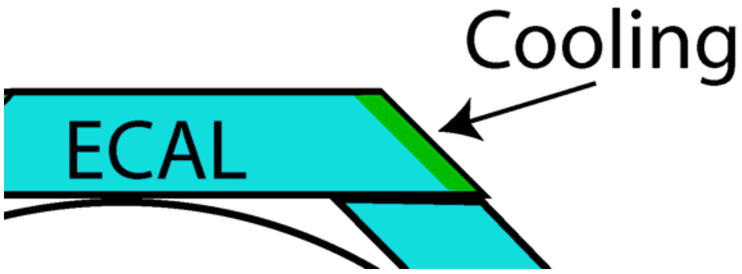
Phase	Current (mA)	Instantaneous Power (mW)	Time begin (us)	Time End (us)	Duty Factor	Average Power (mW)
All Analog "on"	370	930	0	9	0.00108	1.0
Hold "on", charge amp off	85	210	9	100	0.01092	2.3
Analog power down	4	10	100	8333	0.988	9.9
LVDS Receiver, etc		3	0	8333	1	3.0
Decode/Program		10	1	100	0.01188	0.1
ADC		100	10	500	0.0588	5.9
Readout		50	500	2500	0.24001	12.0
Total	459	1313				34.2

- < 40 mW per wafer (~10^3 pixels)

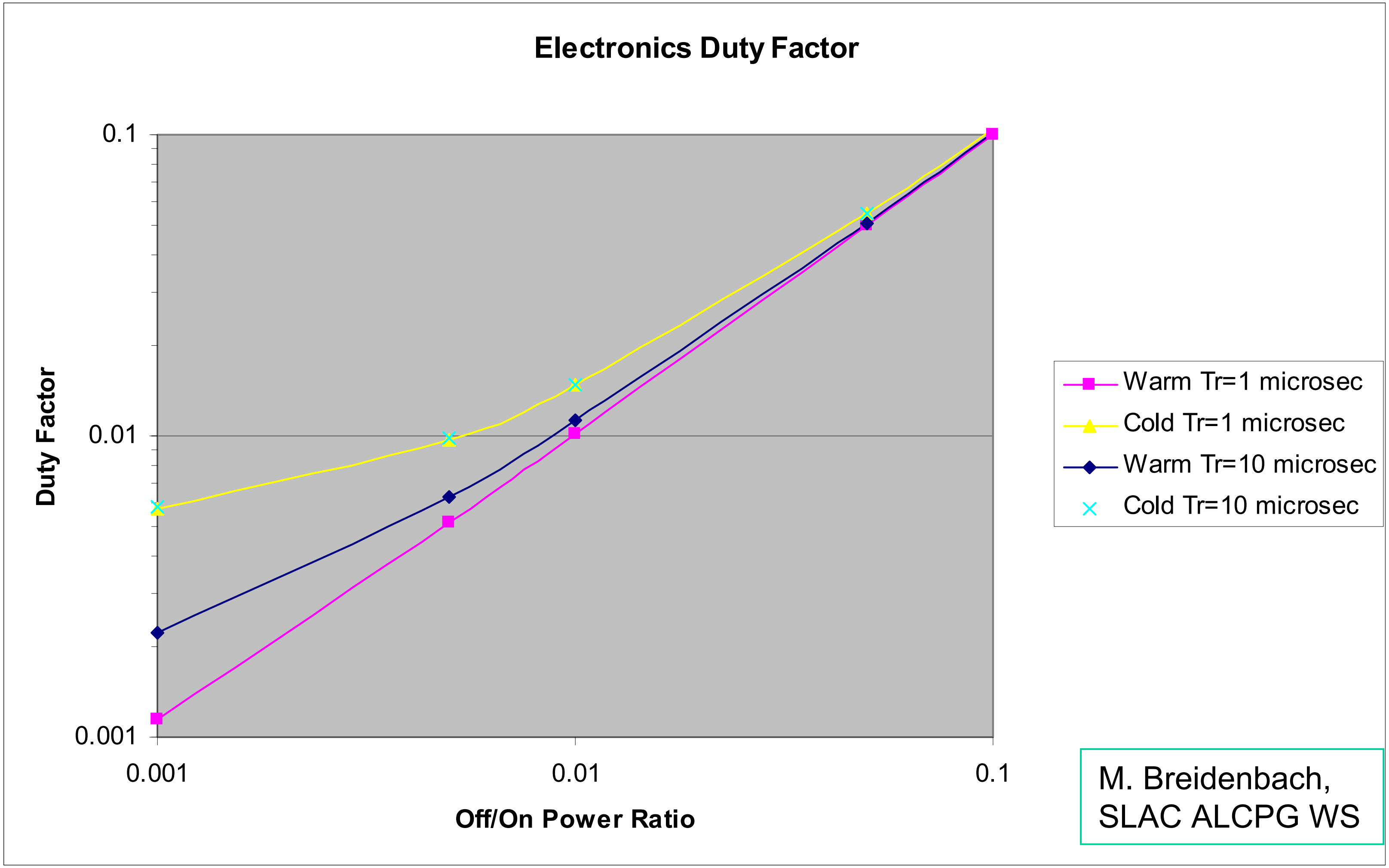
⇒ Passive cooling by conductance in W to module edges

  - ΔT≤ 5° from center to edge

⇒ Maintains small gap & Moliere radius

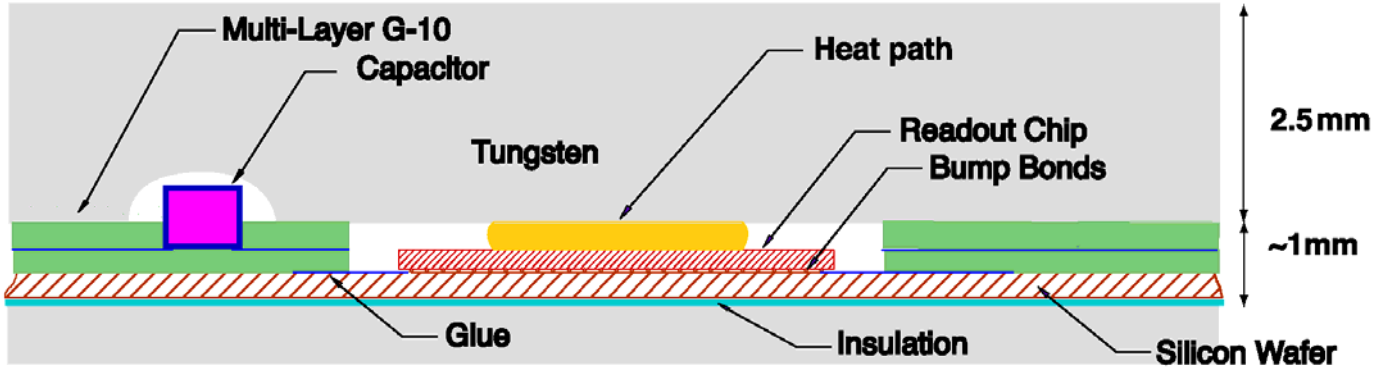


Power (contd.)



- Even though accelerator live fractions are 3×10^{-5} (warm) and 5×10^{-3} (cold), current electronics design parameters give small difference

Maintaining Moliere Radius

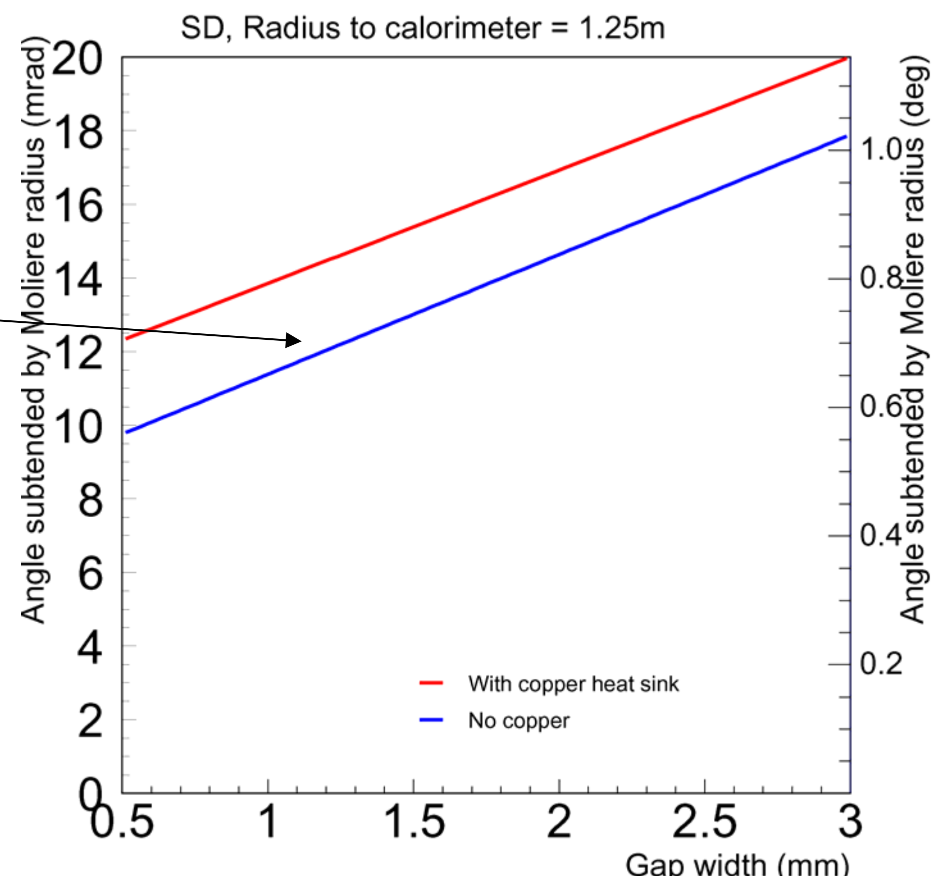


- Shouldn't need copper heat sink if present heat load estimates are correct (or close to correct).

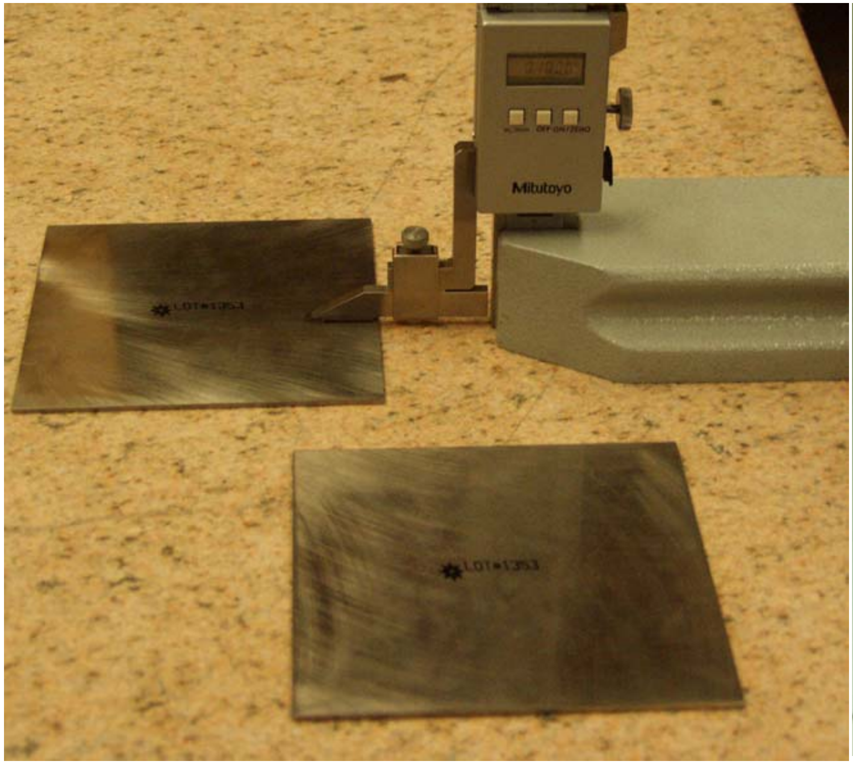
  Angle = 11 mrad
- Compare with effective Moliere radius of 3mm at 1.7m (CALICE?):

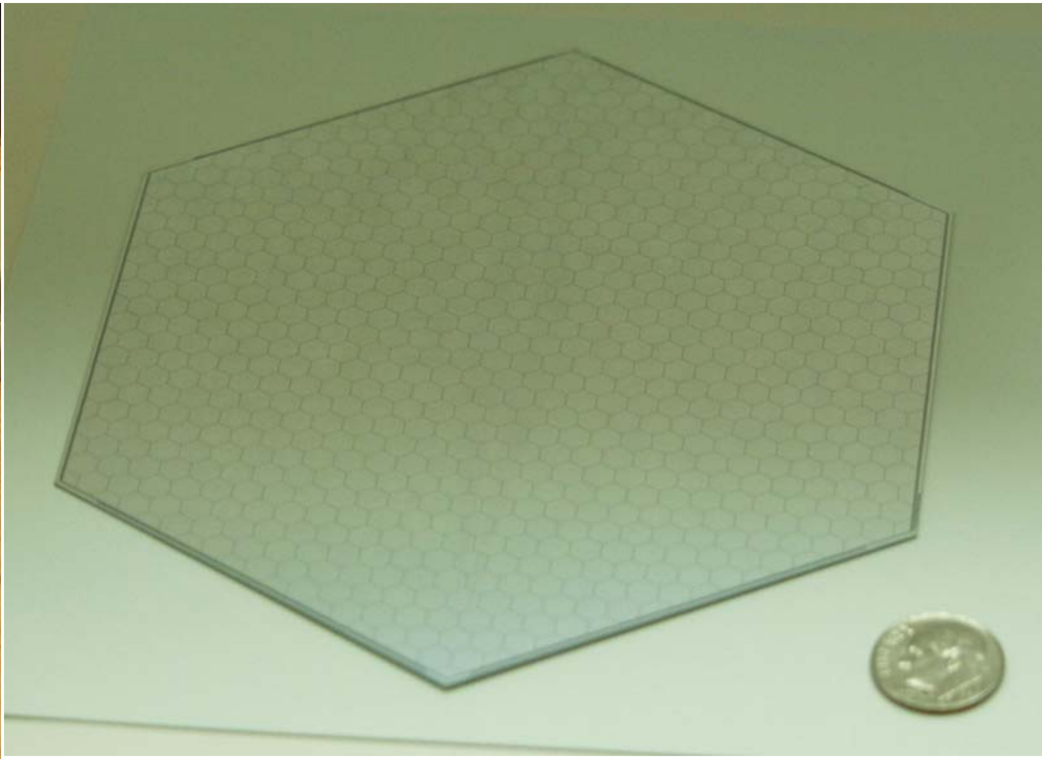
  Angle = 13 mrad

- Capacitors may be biggest challenge



Components in hand





<u>Tungsten</u>

- Rolled 2.5mm
  - 1mm still OK
- Very good quality
  - < 30 µm variations
- 92.5% W alloy
- Pieces up to 1m long possible

<u>Silicon</u>

- Hamamatsu detectors
- Should have first lab measurements soon
- (Practicing on old 1cm dets.)