REPORT ON UK CCD VERTEX DETECTOR R&D

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Oxford University → QMUL

- **Thin ladder studies:**

  CCD thinning experiments

  Unsupported thin ladder prototypes

  FEA studies of supported thin CCDs

- **Fast readout studies:**

  50 MHz readout of CCD58

  Prototype column-parallel r/o CCD

- **Summary**

DESIGN CHALLENGES

Item	SLD	LC	factor
longest CCD (mm)	80	125	1.6
largest CCD area (mm^2)	1280	3000	2.3
# ladders	48	64	1.3
# pixels (M)	307	900	3
ladder thickness (% X_0)	0.4	0.06	6.7
pixel r/o rate (MHz)	5	50	10
column-parallel r/o		$\surd$	1000

+ higher radiation tolerance w.r.t. neutrons

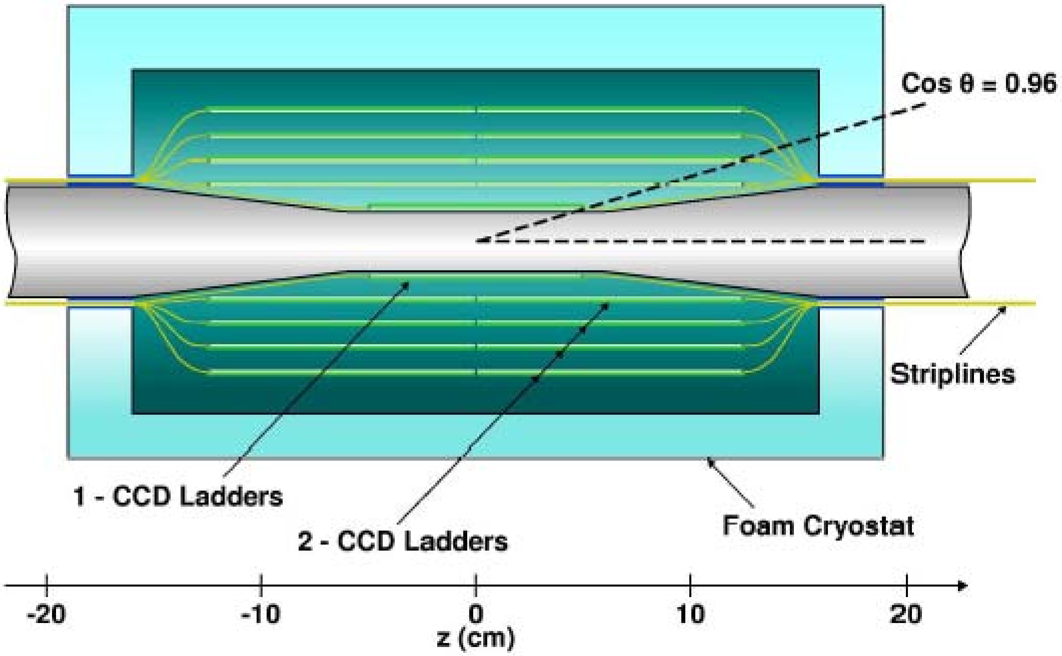
+ compatibility with detector solenoid + RF pickup

R&D PROGRAMME 2001-2006

- Mechanics + cryogenics — Oxford, RAL
- Radiation damage studies — Liverpool
- CCD design + simulations — Marconi
- Driver IC
  Readout IC
  System electronics + DAQ — RAL
- Detector design $\Rightarrow$ physics studies — Bristol, RAL

LCFI vertex detector R&D

Develop ultra-fast CCD vertex detector for the future Linear Collider



- Pixel size ≈ 20 μm square
- Inner layer CCDs: 100×13 mm^2
- Outer layers: 2 CCDs with size 125×22 mm^2
- 120 CCDs, 800×10^6 pixels total
- Very fast readout ≈ 50 μs
- Thinned CCDs: down to 20 μm

Detector Mechanics

Development of thin ladders for detector support

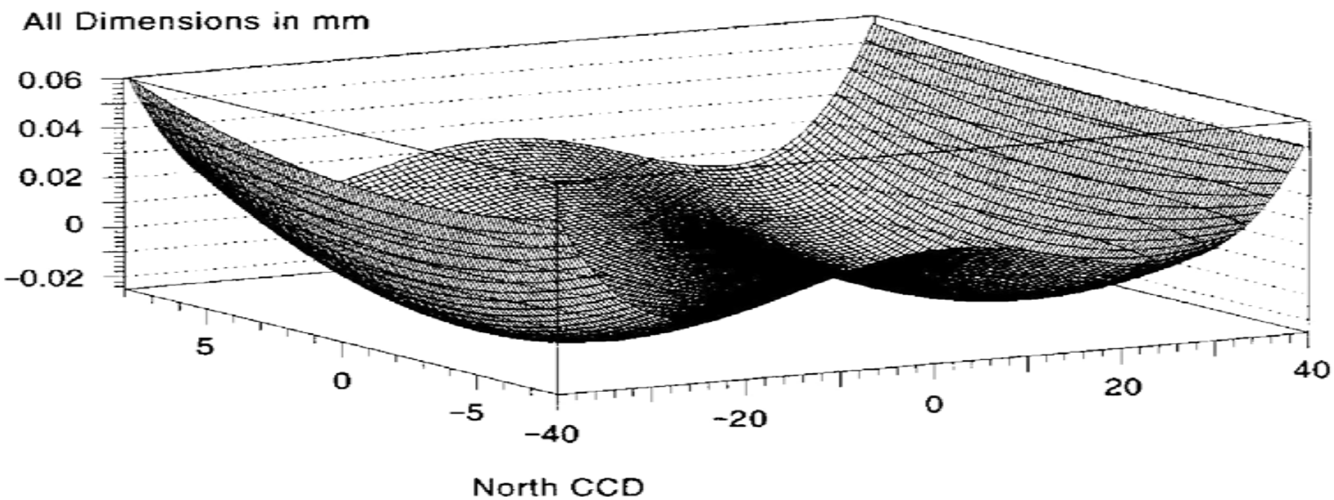
Three options:

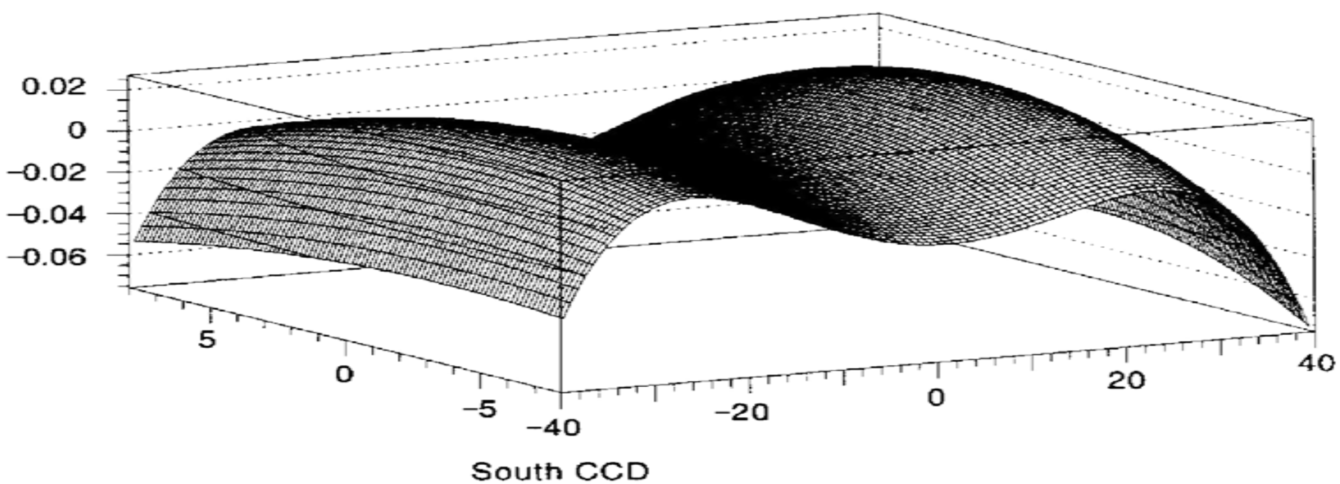
1. Unsupported silicon, thinned to ≈ 60µm and held under tension;
2. Semi-supported CCD (≈ 20 µm thick) glued to thin (and not rigid) support, held under tension;
3. Supported - 20 µm thick CCDs glued to rigid support.

A lot of experience gained on the unsupported version:

- Extremely thin, lowest possible radiation length;
- Precision along the detector length within few microns achieved by tensioning;
- Tension does not rectify bowing across the detector width;
- Semi-supported version should be better in terms of handling and shape distortions.

Distortions of VXD3 CCDs

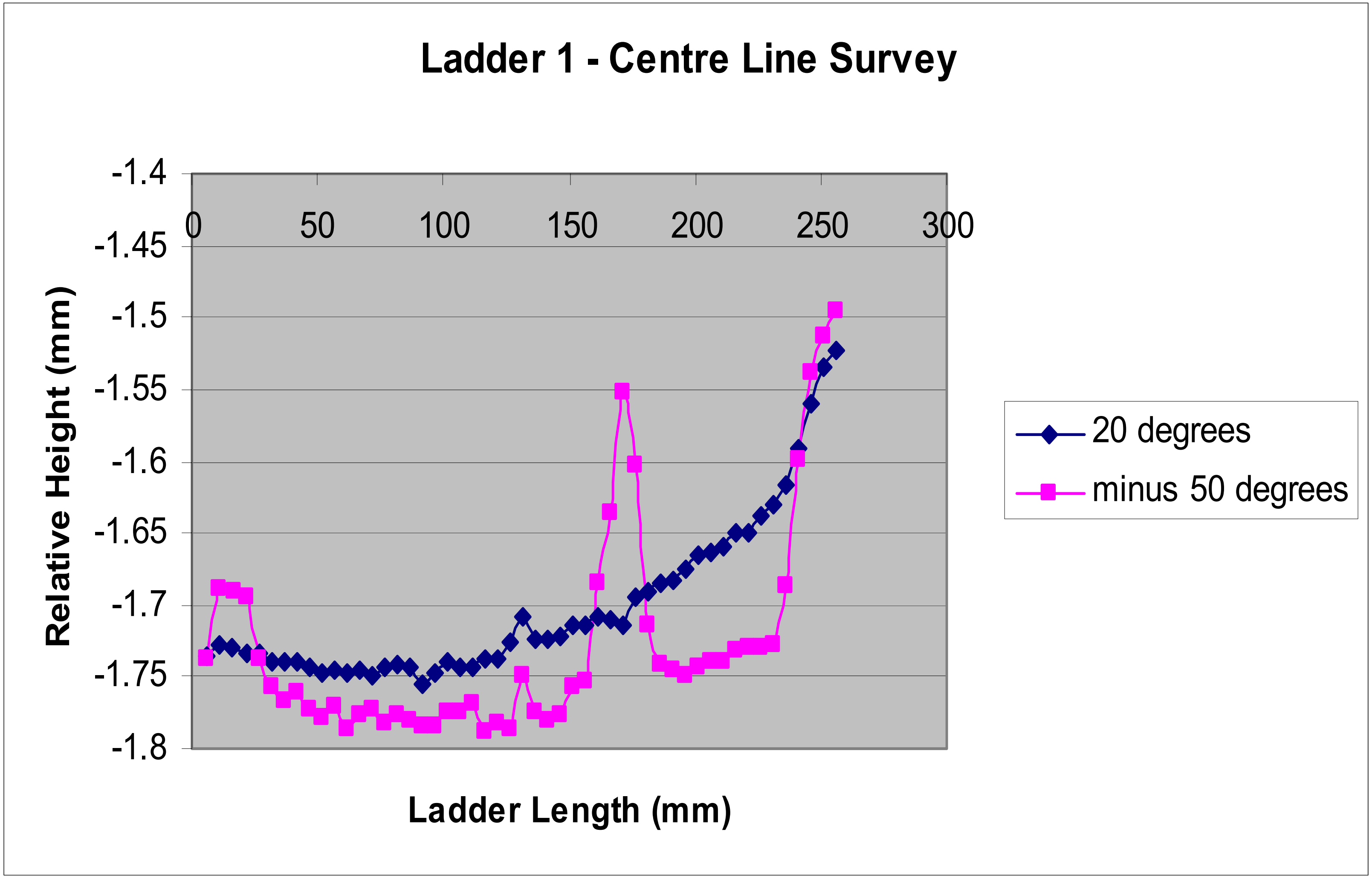




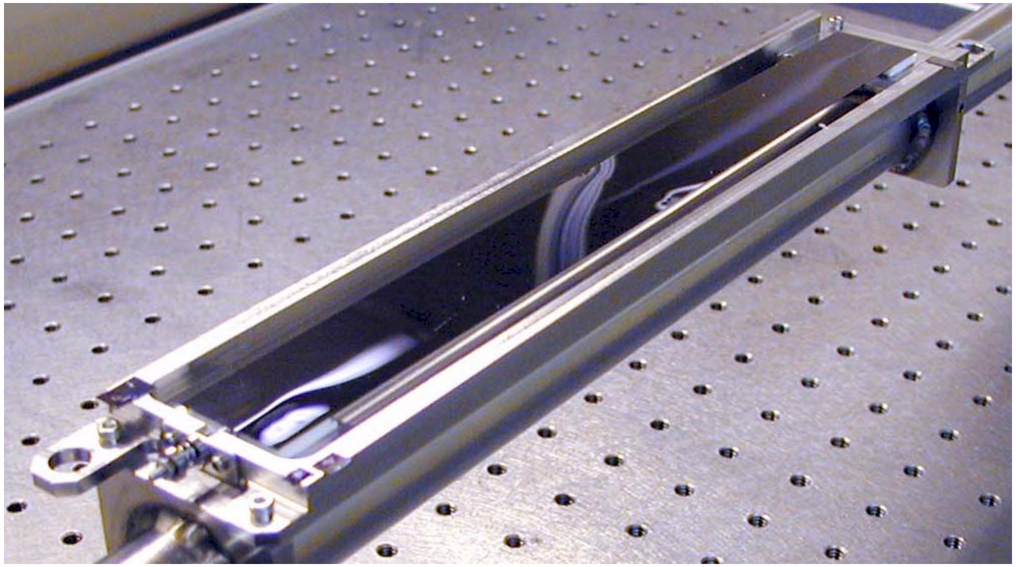
Prototype Ladder Construction

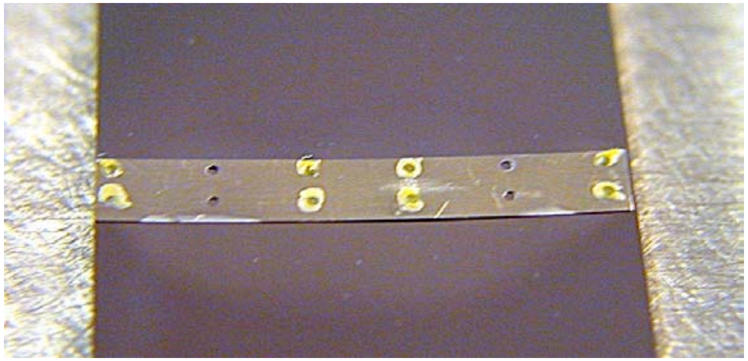
- First prototype ladder made from 60 micron thick unprocessed silicon
- Lesson learned from cold survey
  - Need all blocks, jigs, and ladder master to be flat to as high degree- re-machined
  - Assembly in ‘clean’ environment - blocks and assembly jigs cleaned with nutracon and de-ionised water before use
  - Too much glue causes stresses on the ladder due to greater thermal contraction - glue spot size minimised and precisely controlled using glue dispenser
- Small wells machined into ladder blocks for adhesive so that ladder could remain flat against block
- Need for high temperature glue identified - bump bonding

First Prototype Ladder



Second Prototype Ladder





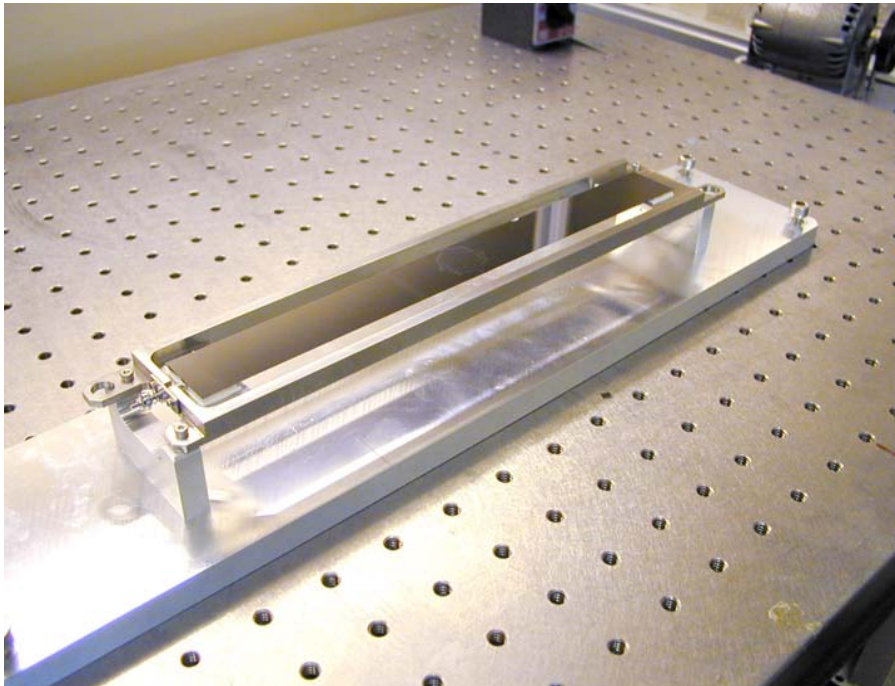
- Glue selected (strain gauge adhesive) required a heat cure at 100°C
- Connector strip made from stainless steel with holes drilled through to minimise material between ladder and support.
- Differential expansions on curing deformed ladder
  - induced curvatures

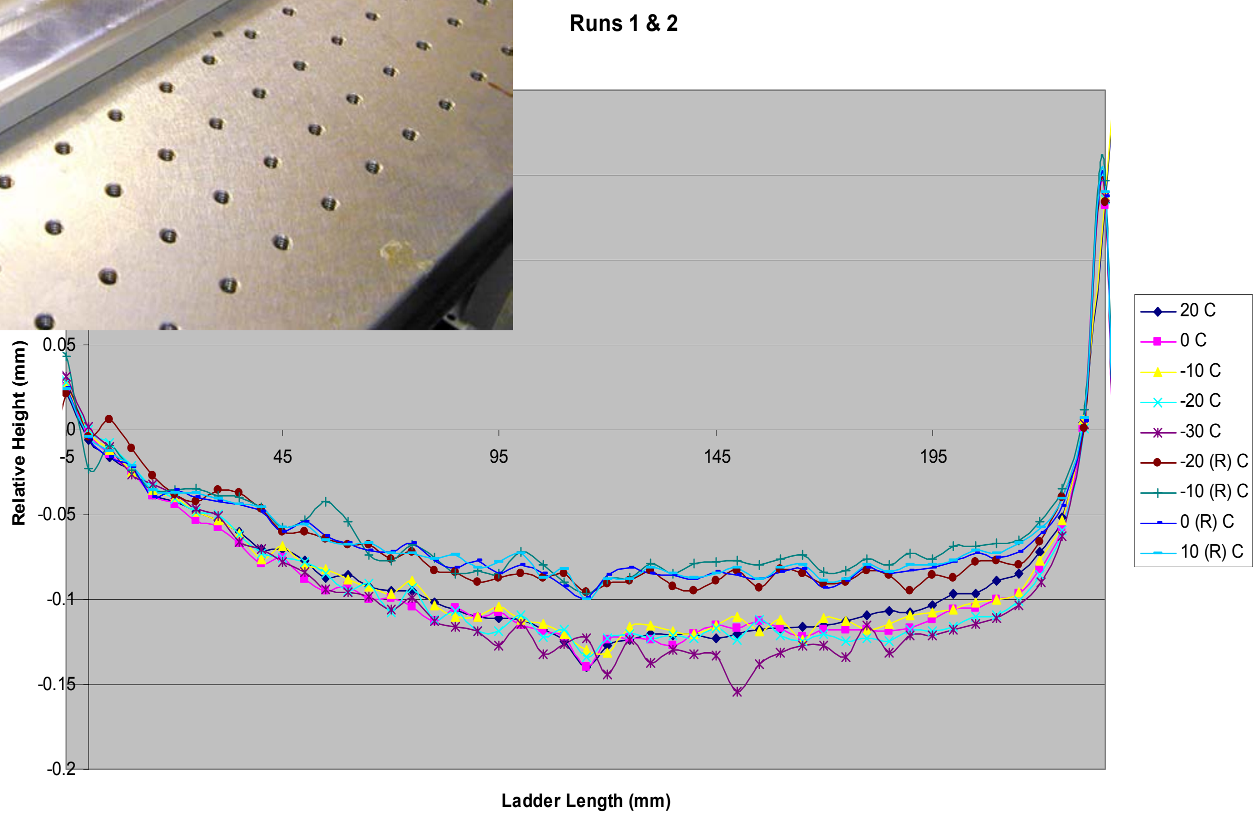
Third Prototype Ladder

- To eliminate CTE mis-matches:
  - Use silicon connector strip with laser cut holes
  - New ladder block structures comprising shapal-M ladder blocks attached with NuSil to 250 micron silicon blocks, then glue to silicon ladder using RT cure glue with 60 micron spacers.

- Overcame problems with previous ladders but now observe a hysteresis effect between heating and cooling the ladder
  - Caused by difference in total force experienced on the ladder due to tension and frictional forces between sliding blocks

Third Ladder Prototype





Hysteresis effects

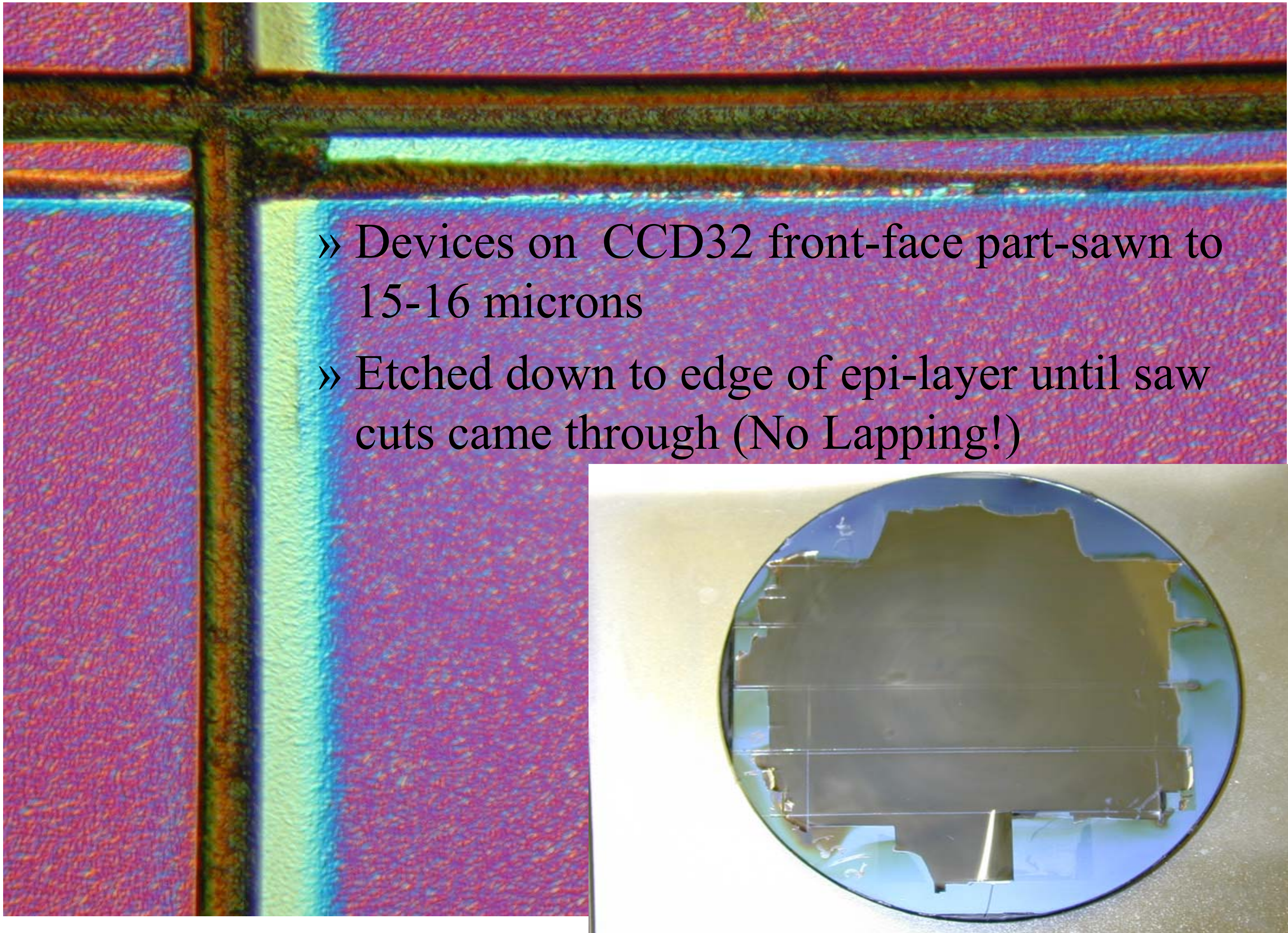
Results of CCD Thinning Experiment at MTech

Glenn Christian,

Andy Harris, Peter Pool (MTech)

Aim: To characterise distortions of thinned CCDs and investigate technique of part-sawing before stop-etching

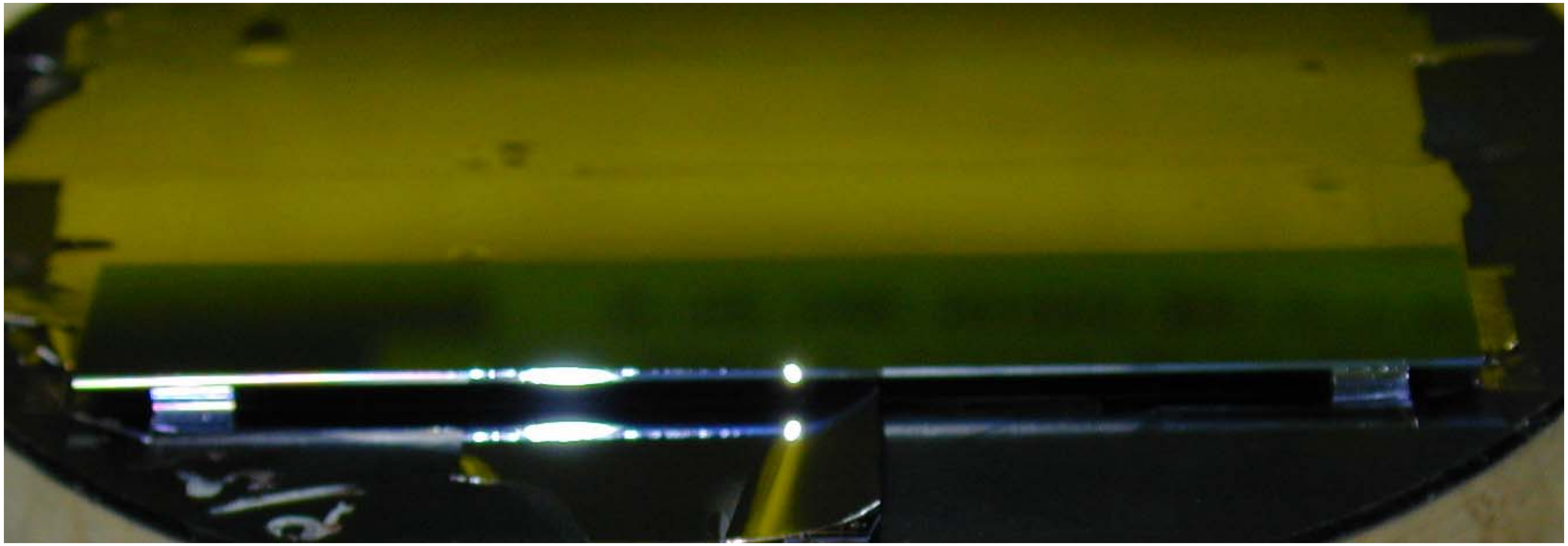
Procedure



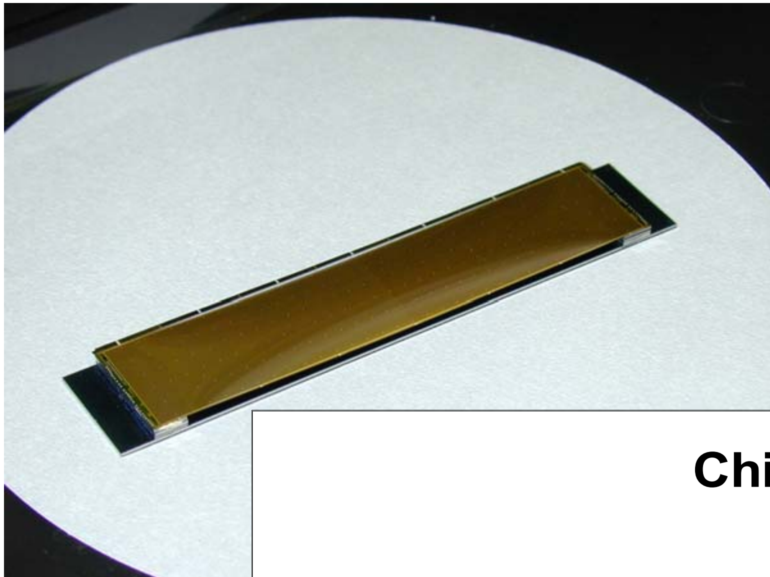
- » Devices on CCD32 front-face part-sawn to 15-16 microns
- » Etched down to edge of epi-layer until saw cuts came through (No Lapping!)

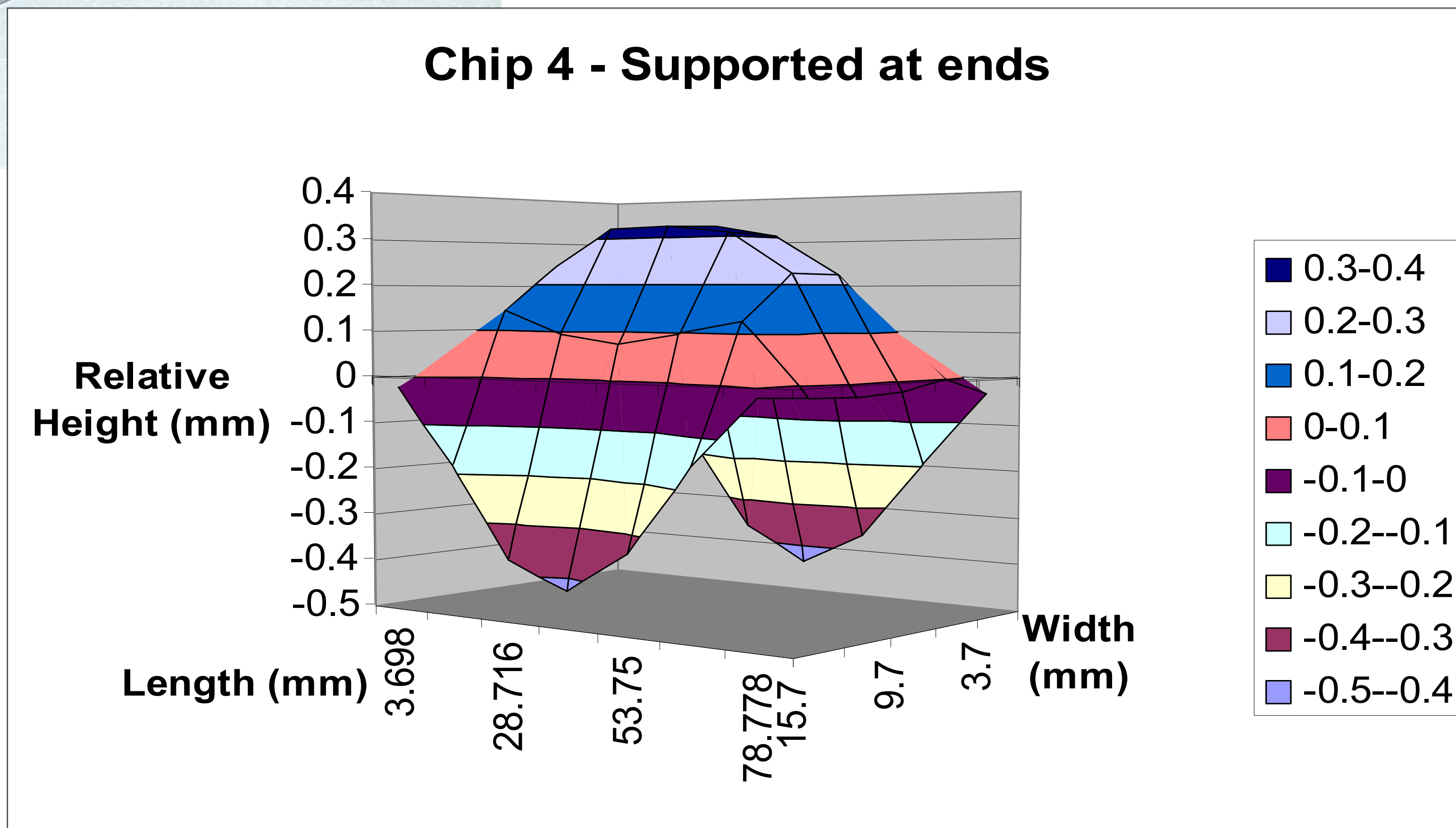
Procedure (continued)

- 3 devices removed from substrate wafer unsupported; 1 supported with thick silicon end blocks and bridge
- Devices removed by melting wax between active and substrate wafers and sliding off
- Residual wax removed in trike bath



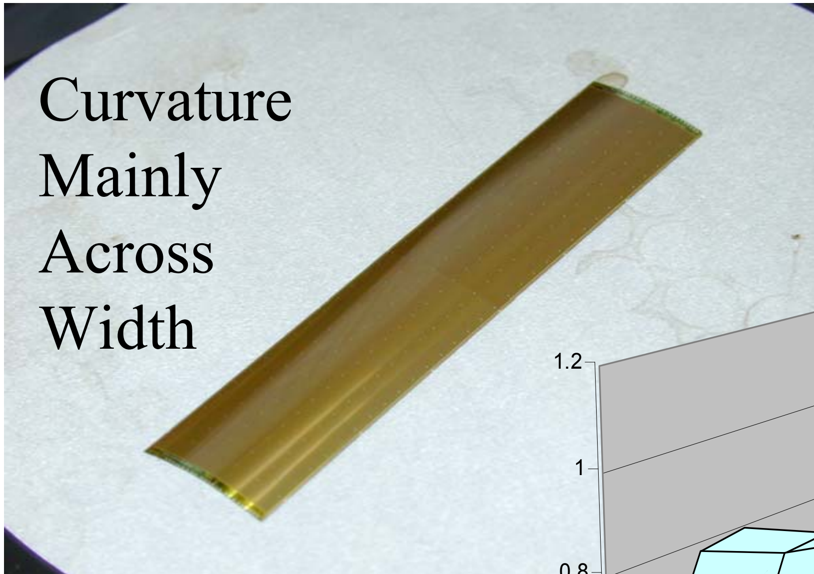
Fourth chip off wafer -Supported at ends c.f. 'unsupported silicon option'

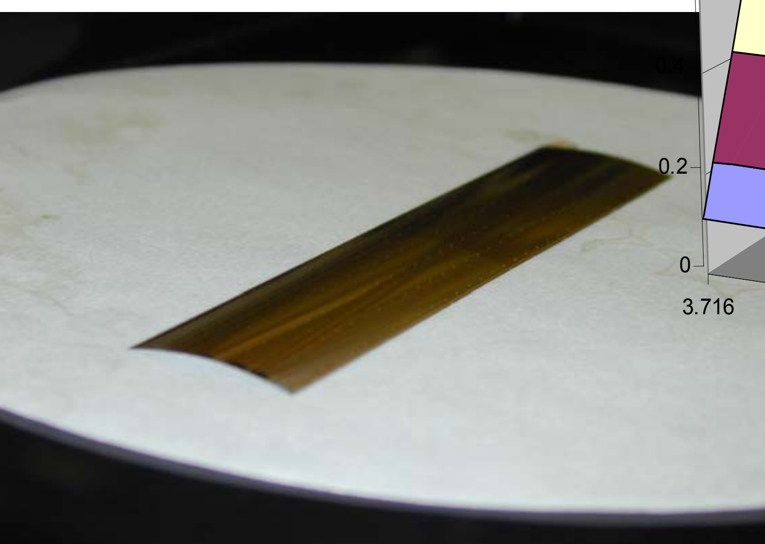


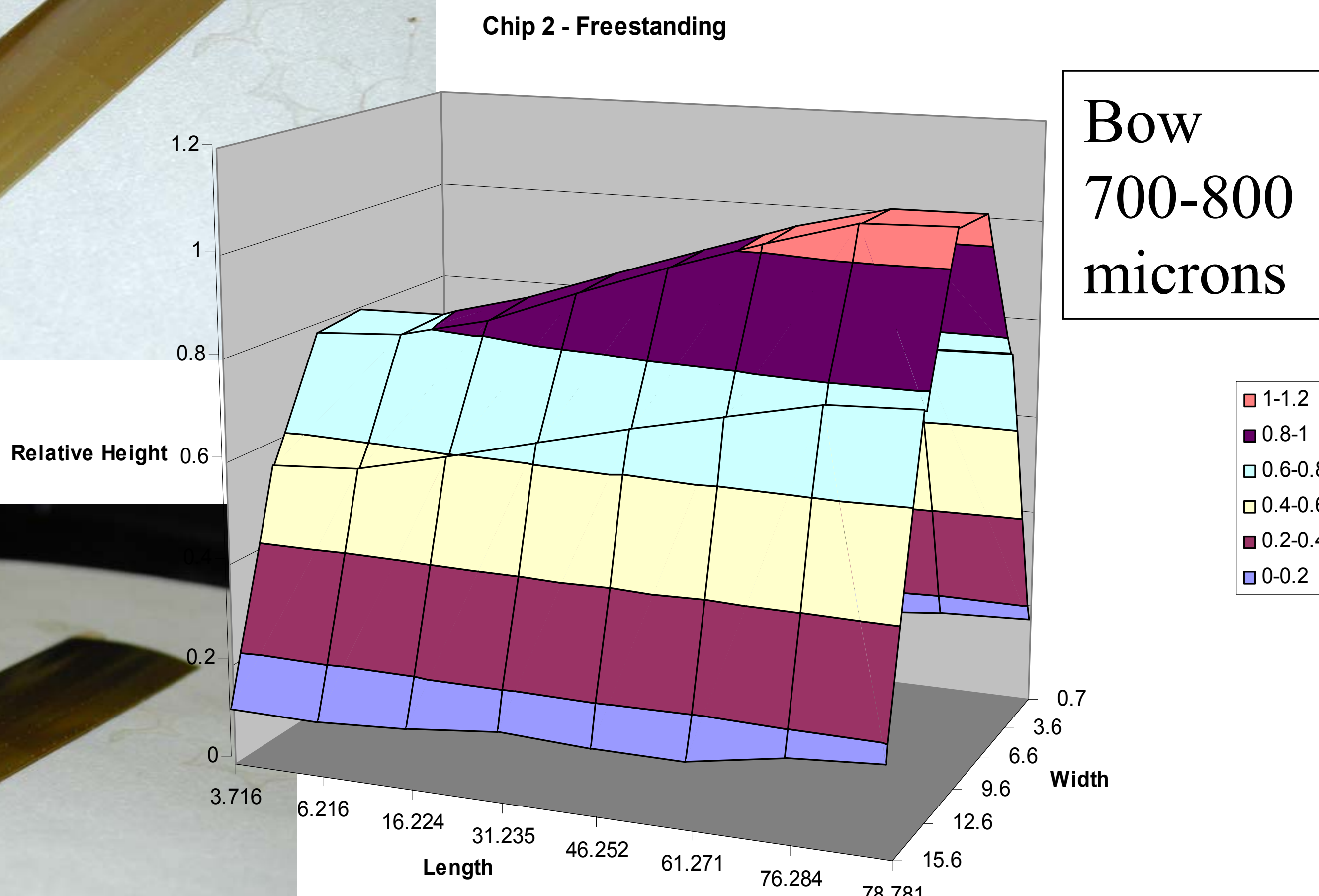


Second chip off wafer
-Completely freestanding

Curvature
Mainly
Across
Width





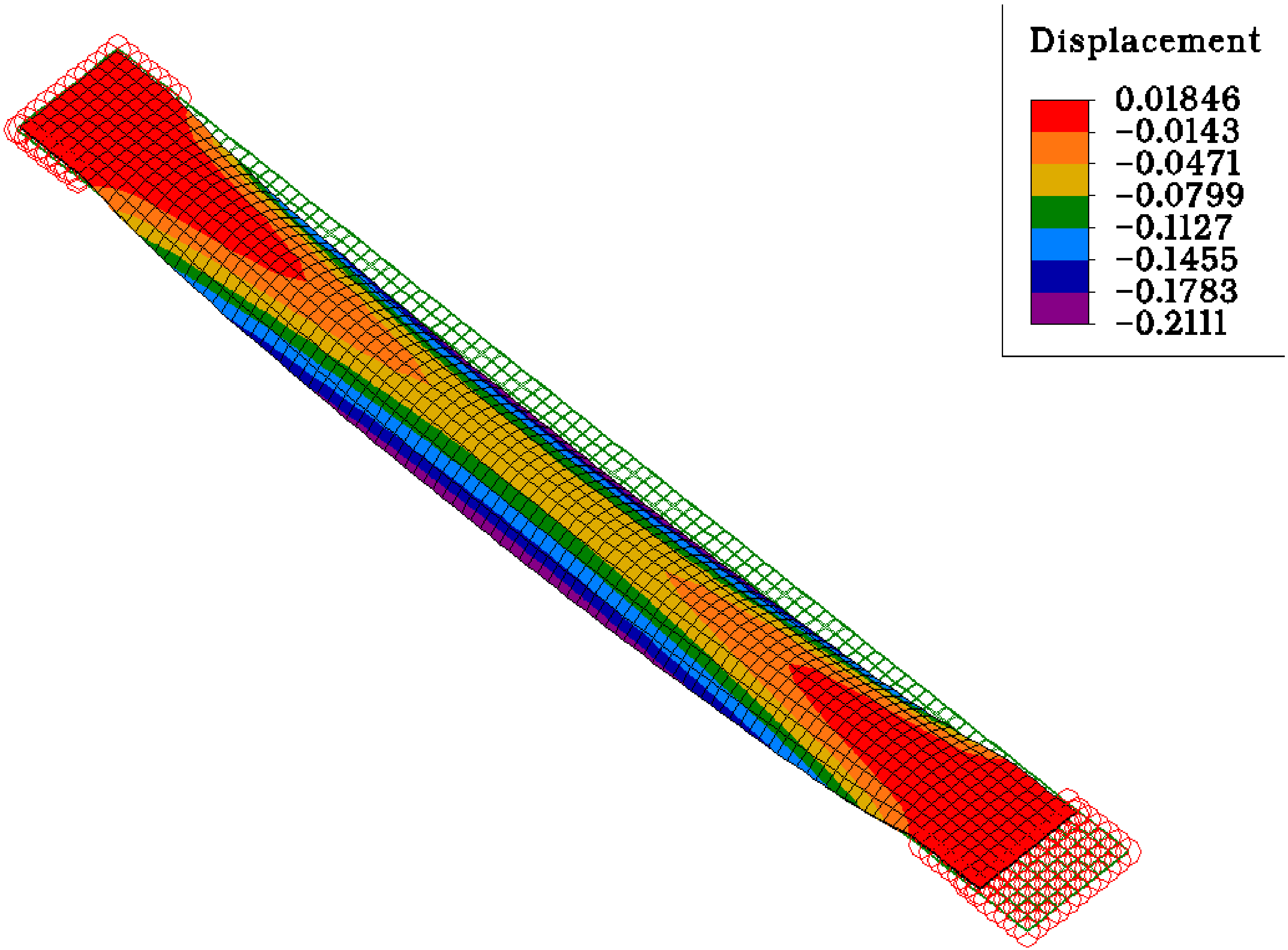


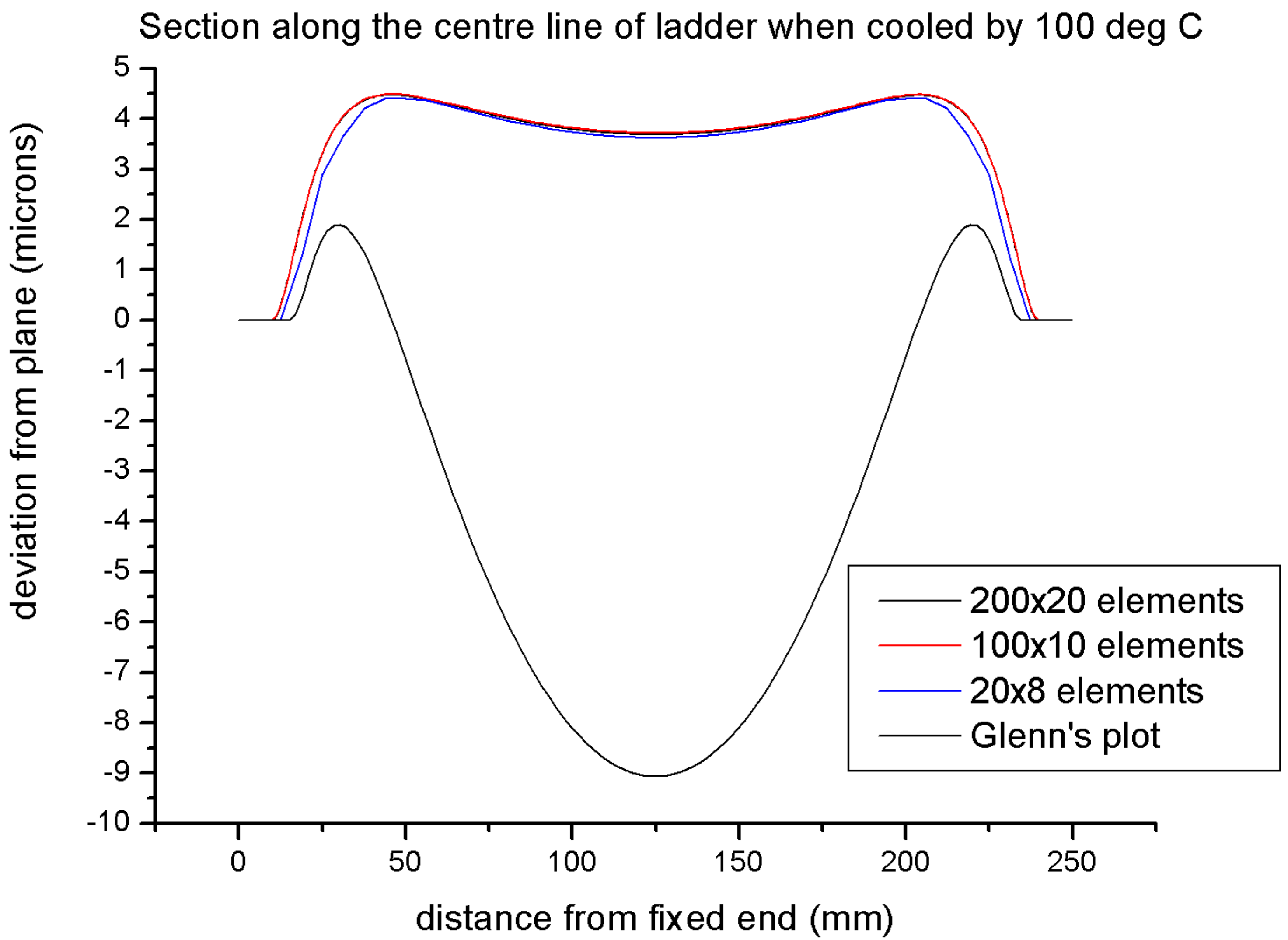
Bow
700-800
microns

Note: Non-linear scale along length

Results

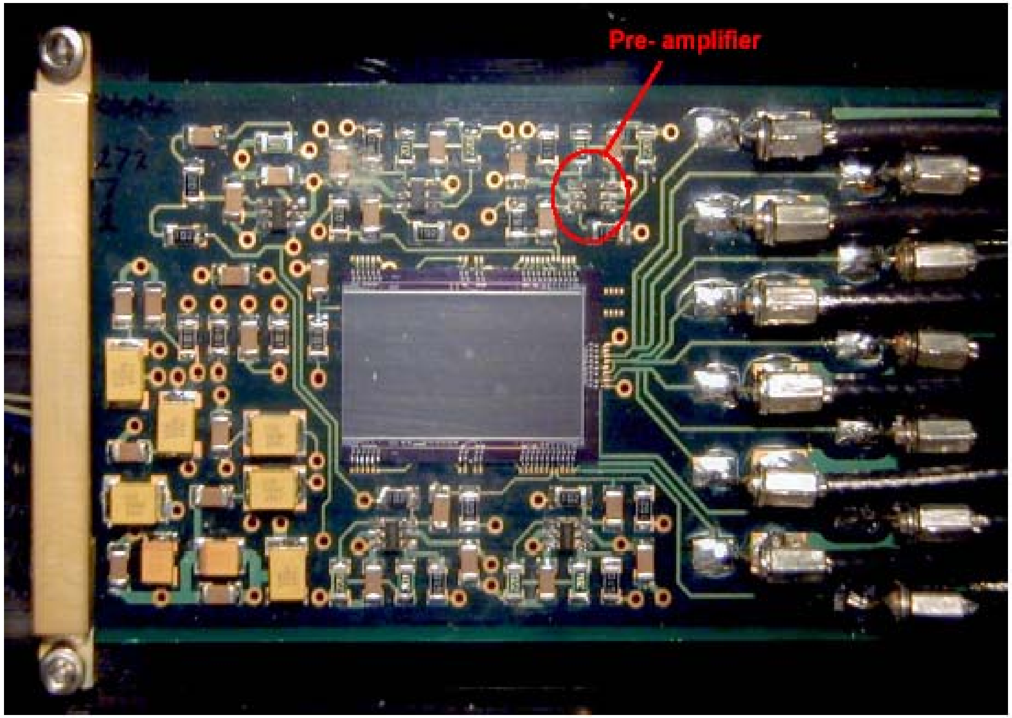
- Final epitaxial thickness – 12-13 microns
  - Etched further into epitaxial layer than planned
- All 4 devices showed bow along width as opposed to length
  - caused by stresses induced from polysilicon electrodes with run across width, probably preventing any longitudinal curl.
- DC probe tests on devices: Passed!
  - Original reason for wafer rejection unknown


Displacement
0.01846
−0.0143
−0.0471
−0.0799
−0.1127
−0.1455
−0.1783
−0.2111



Section along the centre line of ladder when cooled by 100 deg C
deviation from plane (microns)
distance from fixed end (mm)
5
4
3
2
1
0
-1
-2
-3
-4
-5
-6
-7
-8
-9
-10
0
50
100
150
200
250
200x20 elements
100x10 elements
20x8 elements
Glenn's plot

Tests of High-Speed CCDs



Marconi CCD58

- 3-phase, frame transfer CCD
- 2.1 million pixels in 2 sections
- 12 μm square pixels
- Typical signals of interest $\approx$ 1600 electrons
- Low noise $\approx$ 50 electrons at 50 MHz, works down to 3 V_{pp} clocks;
- Readout time at 50 MHz = 25 ms.

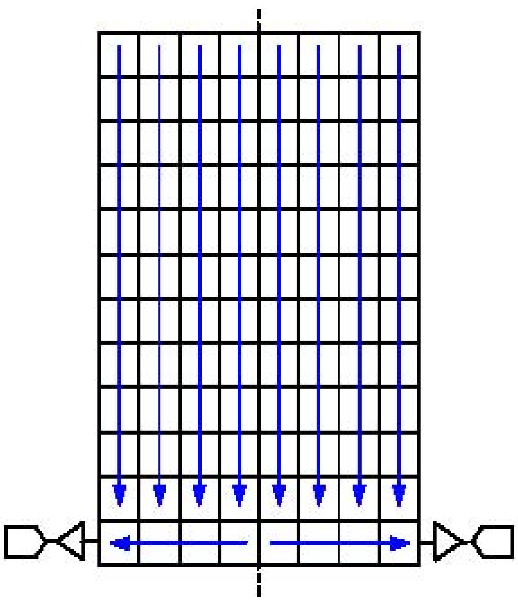
Test bench for high-speed operation with MIP-like signals

Column Parallel CCD

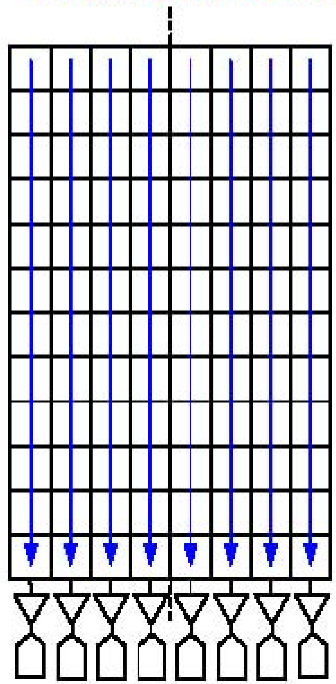
CCD readout time: ≈ 50 μs ➡ 50 Mpix/s from EACH CCD column

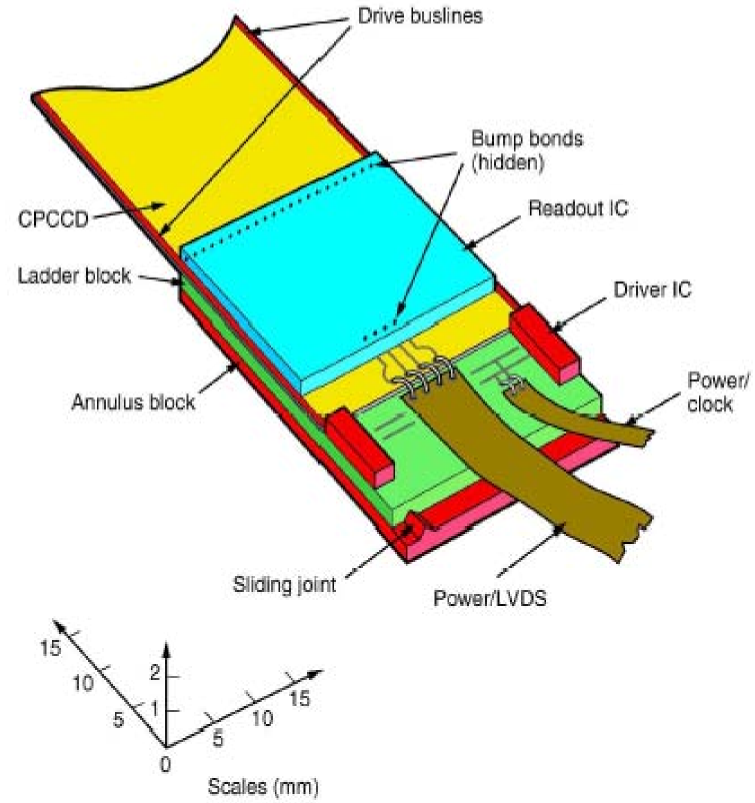
- **Serial register has to be omitted;**
- **Maximum possible speed from a CCD (tens of Gpix/s);**
- **Each column has separate output stage, amplifier and ADC – requires readout chip.**

"Classic CCD"

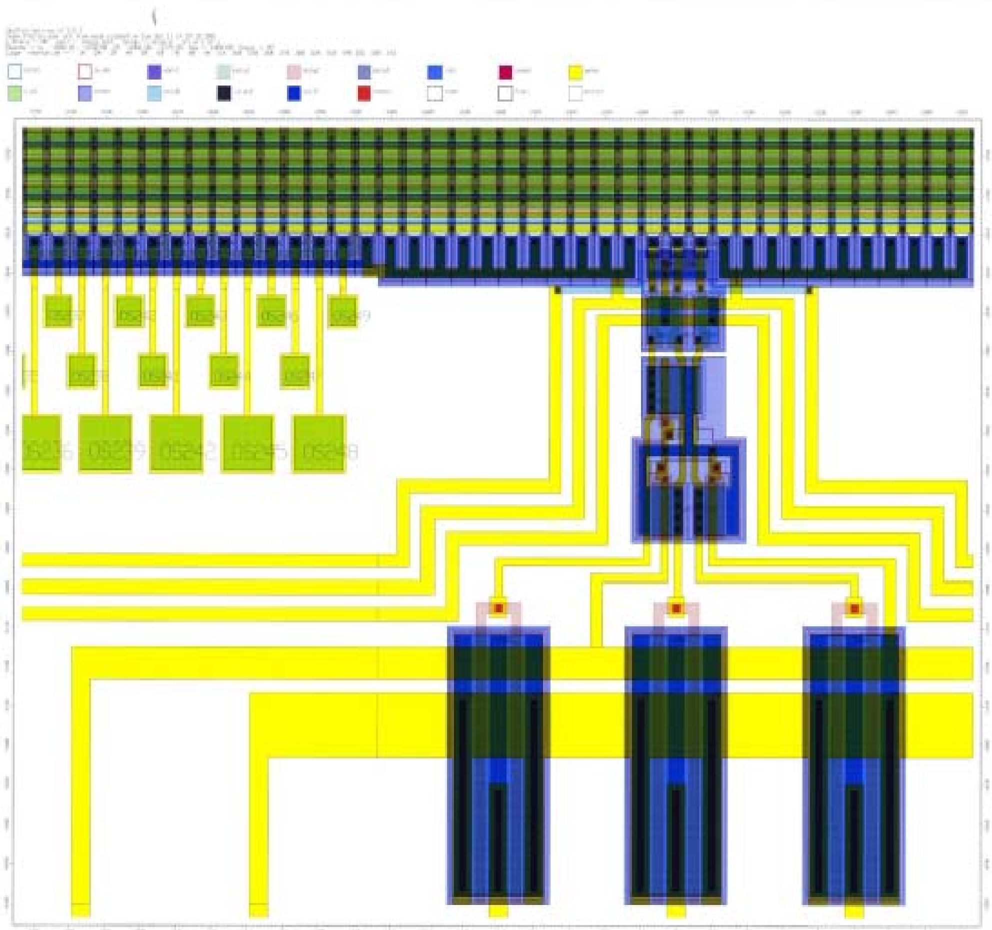


Column Parallel CCD



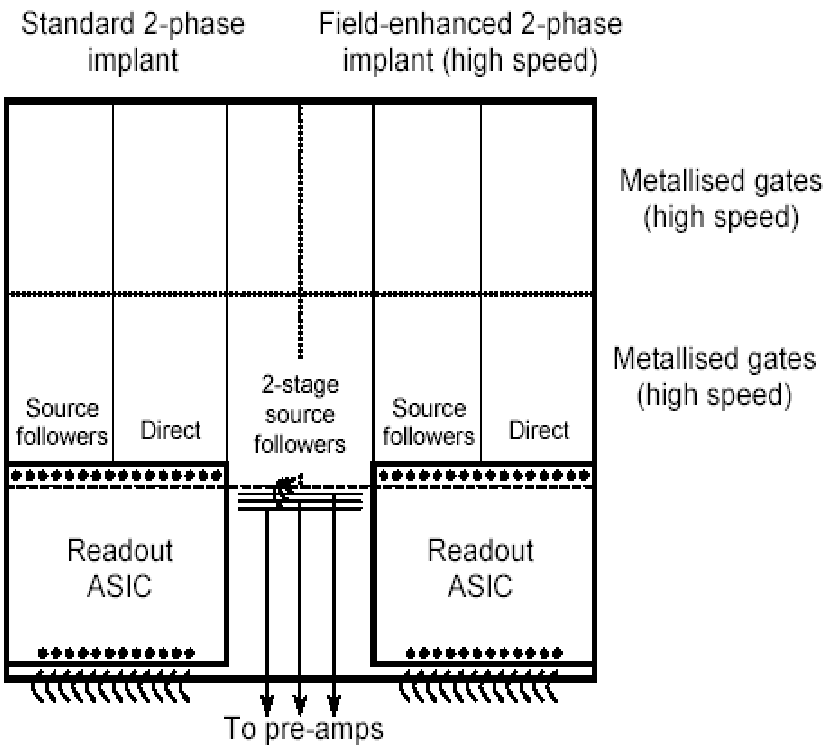


CPCCD design



- Designed by Marconi Applied Technologies;
- Long term collaboration: the same people designed the CCD for VXD3;
- Final design has been completed.
- Ready for production!
- First step in a 5 or 6 stage R&D programme

CPCCD design



- 2 different charge transfer regions;
- 3 types of output circuitry;
- Independent CPCCD and readout chip testing possible;
- Can be tested even if:
  - Bump bonding fails - use wire bonds to readout chip
  - Readout chip fails - use external wire bonded electronics
- Designed to work in (almost) any case.

SUMMARY

Significant progress in past 4 years

- **CCD thinning experiments at Marconi:**

  14μm thick CCDs bow across width!

  $\Rightarrow$ concern for 'unsupported' option

- **4 mechanical ladder prototypes:**

  learning experience: glue, CTE, friction ...

  $\Rightarrow$ Si bridging + room-temp. cure glue OK

  $\Rightarrow$ SLD VXD3 style ladder blocks

- **FEA studies of 'semi-supported' option**

- **50 MHz pixel r/o rate achieved**

  – low noise, lower clocking voltages

- **1st column-parallel device commissioned**