● September, 2002: →

# 3D -- Outline

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→ 4. 3D vs. planar technology, calculations
5. inside the fabrication clean room
→ 6. the keys to 3d fabrication technology
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8. what's on the wafer
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15. an application—protein structure determination
→ 16. fast pulses—x-rays, betas
→ 17. conclusions

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# 3D – A proposed new architecture for solid-state radiation detectors[1]

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ELSEVIER

# Silicon Detectors with 3-D Electrode Arrays: Fabrication and Initial Test Results

Christopher Kenney, Sherwood Parker, *Member, IEEE*, Julie Segal, and Chris Storment

*Abstract*—**The first three-dimensional detectors with n and p electrodes that penetrate through the silicon substrate have been fabricated. Some expected properties, including low depletion voltages, wide voltage plateaus before leakage current limits are reached, and rapid charge collection are reviewed. Fabrication steps and initial test results for leakage currents and infrared signal detection are covered. The authors conclude with a description of current work, including fabrication of active-edge detectors, ones with sensitive areas that should extend to their physical edge.**

*Index Terms*— **Active edges, semiconductor detectors, silicon detectors, three-dimensional.**

## I. Introduction

SOLID-STATE semiconductor diode detectors were developed in 1949 [1] but did not become important for high-energy physics until the development of the microelectronics industry provided rapid advances in their technology. The first wave of improvements was to the detectors themselves, with the use of diffused junctions and oxide passivation [2]–[4], photolithography [5], [7], high-resistivity silicon [6], and getters [7]. The first devices which provided micron-level position information became possible as a consequence of the industry drive to fit ever-larger numbers of ever-smaller transistors on a single chip and of charge transfer devices primarily developed for optical applications [8]–[11]. The development of the first custom very large scale integration (VLSI) readout chip [12] was the key step that made the use of silicon microstrip vertex detectors possible at colliders and much easier in fixed target experiments. However, increasing radiation hardness and speed requirements at a number of new colliders are placing difficult, if not impossible, demands on the best this technology can offer.

Detectors with three-dimensional (3-D) electrodes penetrating into the substrate, such as shown in Fig. 1, should have the capability of satisfying these stringent requirements. Such devices cannot be made by the methods of standard VLSI planar technology, which have been used up to now to make strip and pixel detectors (as well as all current VLSI electronics), since neither ion implantation nor diffusion can alter the silicon more than a few microns below the surface.

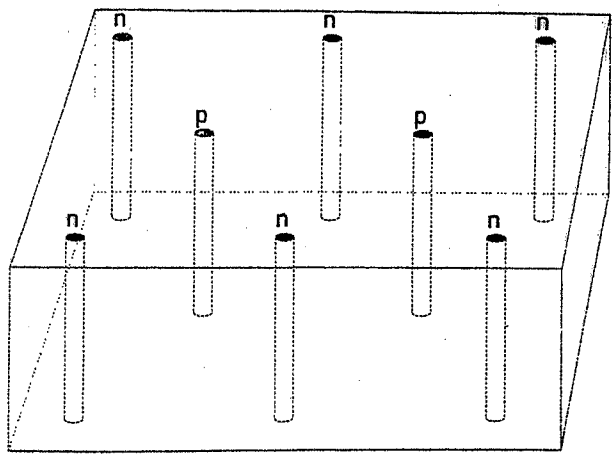


Fig. 1. Three-dimensional view of part of a detector with 3-D electrodes penetrating the substrate.

This paper and two earlier ones [13], [14] describe the beginning of what may be the next step beyond the existing planar detector technology—combining VLSI fabrication technology with the use of additional tools and techniques from the growing field of micromachining to make devices with structures no longer confined to the detector surfaces. Deep holes can now be etched, doped, and filled using these techniques.

The maximum drift and depletion distances are then set by the electrode spacings rather than the detector thickness. Both depletion voltages and collection times can then be kept small. (See Figs. 2 and 3.) Simulations of 3-D detector designs indicate the initial depletion voltages will be in the range of 1 to 10 V, depending on electrode diameter and pitch, and remain low, even with bulk radiation damage that increases the effective doping by a factor of ten. Peak fields, located where the depletion region borders the highly doped electrodes, are an order of magnitude below breakdown levels and can actually decrease under radiation, as a larger fraction of the voltage appears across the increasingly highly doped bulk.

Details of these calculations and some results are given in [13] and [14]. The calculations for the 3-D arrangement use the two-dimensional (2-D) finite element program, MEDICI [15], which also handles such aspects of charge motion as drift, diffusion, and Ramo's theorem effects [16], [17]. The calculations for the planar detector pulse shown in [18, Fig. 3] assume a zero-rise time amplifier to correspond with the amplifier-independent calculation in MEDICI.

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# Observation of Beta and X Rays with 3-D-Architecture Silicon Microstrip Sensors

Christopher J. Kenney, Sherwood I. Parker, Brad Krieger, Bernhard Ludewigt, Tim P. Dubbs, and Hartmut Sadrozinski

***Abstract*—The first silicon radiation sensors based on the three-dimensional (3-D) architecture have been successfully fabricated. X-ray spectra from Iron-55 and Americium-241 have been recorded by reading out a 3-D architecture detector via wire bonds to a low-noise, charge-sensitive preamplifier. Using a beta source, coincidences between a 3-D sensor and a plastic scintillator were observed. This is the first observation of ionizing radiation using a silicon sensor based on the 3-D architecture. Details of the apparatus and measurements are described.**

***Index Terms*—Radiation detectors, radiation sensors, semiconductor detectors, semiconductor sensors, silicon sensors, three-dimensional, 3-D sensors, (3-D) silicon sensors.**

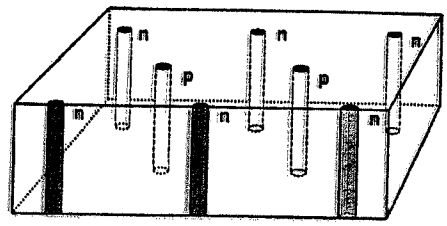


Fig. 1. Schematic, 3-D view of part of a sensor with 3-D electrodes penetrating through the substrate. The front border of the figure is drawn through the center of three electrodes.

## I. Introduction

THE three-dimensional (3-D) architecture for radiation sensors has electrodes that are perpendicular to the wafer's surface, and extend partially or completely through the three-dimensional volume of the wafer. This is in contrast to radiation sensors built using planar technology where the electrode structures are parallel to the surface and restricted to be within a few microns of the wafer's top and bottom surfaces. Fig. 1 shows a schematic view of part of such a sensor, with the front surface in the drawing cut through the middle of three n-type electrodes that penetrate all the way from the top surface to the bottom. Both planar and 3-D silicon sensors use reverse-biased p-i-n diodes, but the electric field in the former is largely perpendicular to the surfaces, while in 3-D sensors, it is parallel. Details on how these devices were fabricated as well as simulations can be found in earlier publications [1]–[3].

There are several properties of planar-architecture radiation sensors that can be improved upon by the incorporation of a 3-D or nonplanar architecture. Among them are the following.

1) At high fluences of interacting particles, radiation damage to the silicon crystal produces damage centers that, in depleted silicon, are charged, increasing the voltage required to fully deplete a silicon p-i-n detector [4]. By allowing the spacing between N and P type electrodes, and hence the depletion distance, to be less than the wafer's thickness, 3-D architecture sensors can be fully depleted after higher fluences than standard planar-architecture sensors [5].
2) Charged particles usually come in parallel to the electrodes, and so all the ionization approaches the electrode, where the induced signal is largest, at nearly the same time. This combined with the short interelectrode distance, produces a large pulse with a fast rise-time.
3) For materials, such as GaAs and diamond, which have significant charge trapping and hence poor charge collection efficiency, the use of a 3-D architecture can reduce the drift path of the signal carriers and hence produce a higher signal-to-noise ratio [6].
4) The addition of active edges [3] should allow the fabrication of sensors with negligible dead volume at the die edges and the seamless tiling of large areas with butted or overlapping sensors.

Earlier results using a pulsed infrared light source [3] indicated that 3-D sensors did deplete at low, reverse-bias voltages as expected. Radioactive sources emitting X rays and gamma rays were then used in this study to demonstrate the ability of the 3-D silicon sensors to detect ionizing radiation. Results of these X-ray measurements and the methods used to achieve them are detailed in the following sections.

## II. Measurements with X and Gamma Rays

The geometry of the sensor used for these measurements was that of a strip detector where sets of twelve, like-type electrodes were tied together to form line segments. Each individual electrode extended completely through the wafer and consisted of a doped polycrystalline silicon core from which dopant atoms have been diffused into the surrounding single-crystal silicon. The separation between electrodes within a strip was 100 $\mu$m, and that between neighboring strips of opposite type was also 100 $\mu$m. The n-type strips alternated with p-type strips in an interdigitated arrangement, with the n-type electrodes midway between the p-type electrodes in the strip direction. Surrounding

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# Performance of 3-D Architecture Silicon Sensors After Intense Proton Irradiation

Sherwood I. Parker and Christopher J. Kenney

*Abstract*—**Silicon detectors with a three-dimensional architecture, in which the n- and p-electrodes penetrate through the entire substrate, have been successfully fabricated. The electrodes can be separated from each other by distances that are less than the substrate thickness, allowing short collection paths, low depletion voltages, and large current signals from rapid charge collection. While no special hardening steps were taken in this initial fabrication run, these features of three-dimensional architectures produce an intrinsic resistance to the effects of radiation damage. Some performance measurements are given for detectors that are fully depleted and working after exposures to proton beams with doses equivalent to that from slightly more than ten years at the B-layer radius (50 mm) in the planned Atlas detector at the Large Hadron Collider at CERN.**

*Index Terms*—**Detectors, pin diodes, radiation hardness, semiconductor detectors, silicon detectors, three-dimensional electrodes.**

## I. Introduction

SINCE the first custom VLSI chip was developed for the readout of silicon strip detectors [1], both the chips and the detectors have been fabricated by planar technology methods. With the precision provided by small strip spacing and the compact readout provided by the VLSI chips, such detectors have played an increasingly important role in tracking at collider detectors.

The coming generation of high-luminosity colliders will subject their innermost detector elements to extreme levels of radiation. Silicon detectors are subject to a number of damage sources.

1) Ionization-caused charging of their surface oxide passivating layers can attract mobile substrate charges. These in turn may short out adjacent electrodes or increase their interelectrode capacitance [2]–[4]. This charging has been seen to saturate at a value of 2.5 $\times 10^{12}$ charges per cm$^2$ for a 500-nm-thick oxide, but with no electric field applied during irradiation [5]. The same paper reported effects attributed to continued charging in the similar oxide of a gated diode (but now subject to an electric field) at fluence values more than five times as high, not an unreasonable result with an electric field driving charge to the surface.

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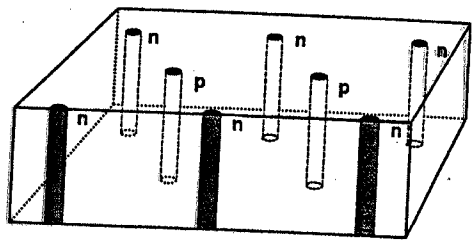


Fig. 1. Schematic, three-dimensional view of part of a sensor with 3-D electrodes penetrating through the substrate. The front border of the figure is drawn through the center of three electrodes.

2) Damage to the crystal lattice produces defects that are negatively charged when the silicon is depleted, causing lightly doped n- and p-type silicon to develop a high depletion voltage of the same sign as that of p-type silicon [6]–[11]. While some of this damage can anneal out, a temperature-dependent reverse annealing can cause a major increase in such damage [12]–[15]. Maintaining the detectors continuously at $-5$ to $-10$ °C prevents this reverse annealing, but if the cooling is ever lost for more than a few days, the damage will be irreversible. A model for this bulk damage, involving divacancies and divacancy-oxygen defects, $V_2O$, has been developed, which explains effective doping changes, leakage current increases, and the leakage current temperature dependence for $^{60}$Co gamma irradiation [16]. Such detailed agreement is not found for hadron interactions, which create dense damage clusters that are not yet understood in detail.
3) The charge carrier lifetime decreases, also from bulk damage [17]–[19]. (In addition, the lifetime was found to vary with bias voltage [20].)

Recent work has shown that the incorporation of about $10^{17}$ oxygen atoms per cm$^3$ increases the fluence, by approximately a factor of two, for a given increase in those negatively charged defects [21]–[24]. This beneficial effect is not present with neutron irradiation, indicating that it may be the damage from the less-dense Coulomb interactions that is being reduced. The incorporation of oxygen also does not seem to reduce leakage currents [25].

This paper describes the first radiation-damage test results for a new form of silicon detector, which has a three-dimensional (3-D) array of n- and p-electrodes perpendicular to the surface and which penetrate the entire thickness of the detector [26]–[29]. Fig. 1 shows a schematic view of such a detector. The low depletion voltages and short collection paths for ionization charges made possible with 3-D technology result in an intrinsic

# Results From 3-D Silicon Sensors With Wall Electrodes: Near-Cell-Edge Sensitivity Measurements as a Preview of Active-Edge Sensors

Christopher J. Kenney, Sherwood Parker, and Edith Walckiers

*Abstract*—**Silicon sensors with a three-dimensional (3-D) architecture, in which the n and p electrodes penetrate through the entire substrate, have been successfully fabricated. The electrode spacing can be less than the substrate thickness, allowing short collection paths, low depletion voltages, and large current signals from rapid charge collection. This paper gives results when the cylindrical electrodes of the earlier papers are replaced by a combination of cylindrical and wall electrodes—ones in which a trench, rather than a hole, is filled with doped polycrystalline silicon. The detection efficiency remains high to within a few micrometers of these wall electrodes, and is an indication that similar high efficiencies should be achievable near the physical edges of the proposed active-edge sensors.**

*Index Terms*—**Active edges, detectors, guard rings, insensitive edge regions, semiconductor sensors, silicon sensors, three-dimensional (3-D) electrodes, 3-D sensors.**

## I. Introduction

SINCE the first custom VLSI chip was developed for the readout of silicon strip sensors [1], both the sensors and their readout chips have been fabricated by planar technology methods, in which all fabricated structures lie within a few micrometers of either surface. These sensors employ silicon diodes with electrodes in the form of closely spaced strips or pixels, with p-type electrodes on one surface and n-type ones on the other. Reverse-biased, they form a depleted diode with an electric field between the p and n electrodes for the collection of ionization charges. This field must be kept away from the saw cuts along the sensor edges, since they, with all their dangling bonds, are conducting and would short it out. Further space is needed to keep the field region from any cracks and chipped regions caused by the sawing. They can reach some tens of micrometers in from the edge. Space must also be left for guard rings, which drop the voltage in a controlled fashion, and intercept edge leakage currents before they reach the instrumented electrodes. For example, all these structures on the Atlas pixel sensors at CERN occupy 14% of the total surface area, not including any material in the saw lanes [2]. Fig. 1 shows a schematic view of the various features that result in significant dead areas along sensor edges. Fig. 2 shows an electron micrograph of a saw cut through four trenches. The sort of damage

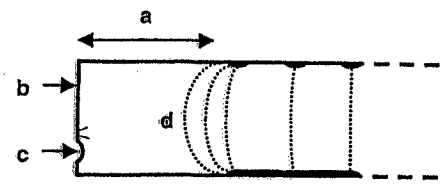


Fig. 1. Schematic cross-section view of a sensor edge, showing some reasons for the insensitive region there: (*a*) space may be needed for guard and voltage-dropping rings, (*b*) the saw-cut edges are conducting, and (*c*) often contain chips or microcracks, all of which must remain clear of (*d*), the bulge of the edge of the electric field in the depleted region.

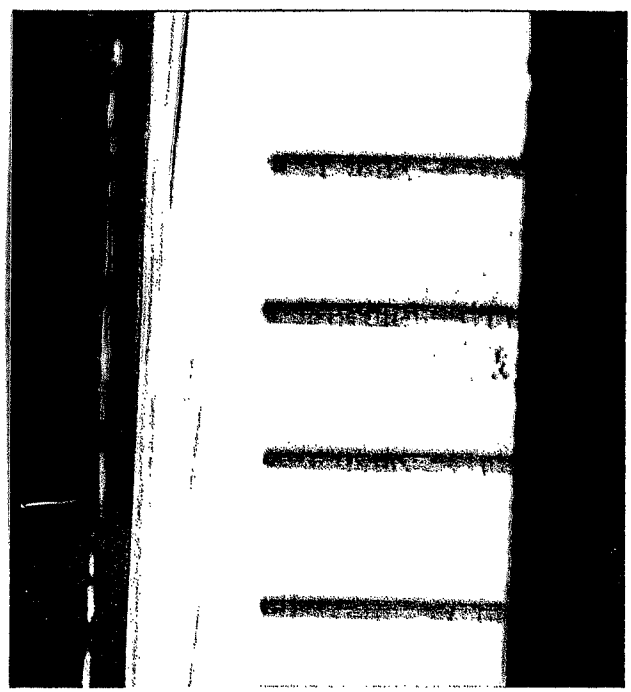

Fig. 2. Photograph of the cross section of a 525-$\mu$m-thick wafer with etched trenches. Damage from the diamond saw wheel, schematically indicated in Fig. 1, can be seen along the right center and left surfaces.

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# Technology development of 3D detectors for high-energy physics and imaging

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**Abstract**

Various fabrications routes to create '3D' detectors have been investigated and the electrical characteristics of these structures have been compared to simulations. The geometry of the detectors is hexagonal with a central anode surrounded by six cathode contacts. A uniform electric field is obtained with the maximum drift and depletion distance set by electrode spacings rather than detector thickness. This should improve the ability of silicon to operate in the presence of the severe bulk radiation damage expected in high-energy colliders. Moreover, 3D detectors made with other materials (e.g. GaAs, SiC) may be used, for example, in X-ray detection for medical imaging. Holes in the substrate were made either by etching with an inductively coupled plasma machine, by laser drilling or by photochemical etching. A number of different hole diameters and thickness have been investigated. Experimental characteristics have been compared to MEDICI simulations. 

*Keywords:* 3D detectors; Semiconductor; Medical imaging; Radiation hardness

## 1. Introduction

The study and quest for new radiation hard silicon detectors has become very active in recent years [1]. Because of their high efficiency, small thickness and fast readout, silicon detectors are widely used in high-energy physics experiments, including future experiments such as those at the Large Hadron Collider (LHC). The LHC will bring proton beams into collision at the centre of the mass energy of up to 14 TeV. The very high luminosity foreseen ($\sim 10^{34}\,cm^{-2}\,s^{-1}$) implies that silicon detectors have to resist hadron fluxes of the order of $10^{13}\,cm^{-2}\,yr^{-1}$.

Under these conditions, detector performance may be limited by a large number of defects introduced into the device. The charge generated by the ionising radiation is trapped in discrete energy levels generated in the band-gap of the silicon substrate, resulting in incomplete charge collection. Moreover, irradiation results in a

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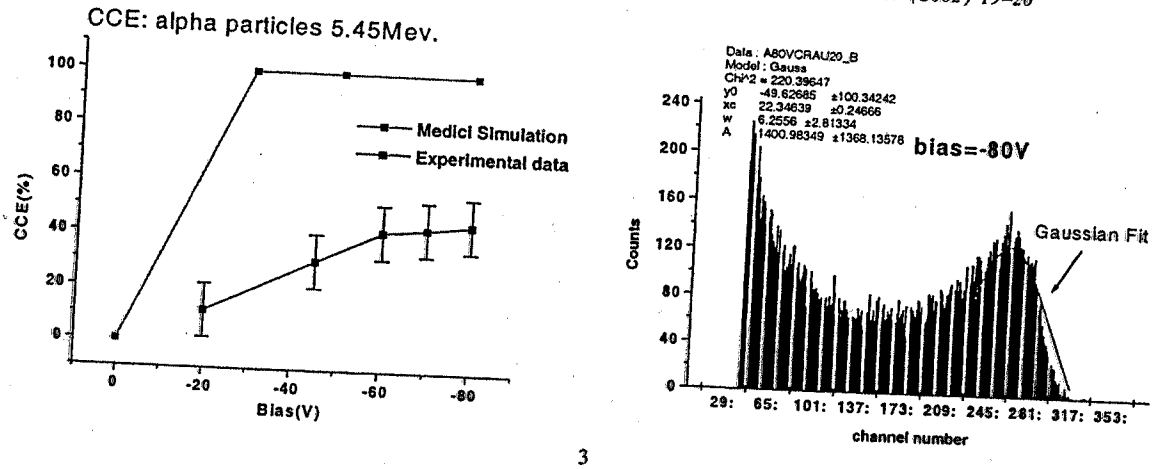



Fig. 3 (*continued*).

Fig. 3(2)d simulations incorporating sidewall damage show good agreement with the experimental data. The principal mechanism that causes deep defects within dry etched material is ion channelling [8]. This occurs when an ion is scattered into the crystal along a low-index direction. When the ion loses energy, it creates point defects and localised defect complexes, depending on the energy.

### 3.1.3. Charge collection measure

α-particle pulse height spectra was measured on the fabricated detectors. For light and electric screening the sample was placed in a metal box which had a hole on one side. An Americium-241 (α-5.45 MeV) source was placed above this hole to irradiate the device. Due to the limited range of α−particles in air, the apparatus was placed in an evacuated metal container at a pressure of about 25 mbar. The signal from the detector was read by an Ortec pre-amplifier connected to a post-amplifier with a 500 ns shaping time. The signal was then processed by a PC-based multi-channel analyser to obtain a spectrum.

Fig. 3(3) shows the spectrum and the CCE curve obtained for a 3D detector dry etched and with Schottky contacts. The charge collected at −80 V is about 50% of the total charge generated by α−particles. This is the maximum value obtained so far. The reason for the charge loss may be the damage induced by the dry etching process. Defects formed inside the bulk semiconductor material, if charged, can screen the electric field generated between the electrodes. Simulations without sidewall damage show that 100% charge should be collected already at −30 V.

## 4. Conclusion

So far 3D detectors using Schottky contacts have been successfully created and tested. Process steps for the fabrication of 3D radiation detectors with Schottky contacts have been developed and complete detectors made. Dry etching, laser drilling and electrochemical etching have been used to create holes in different semiconductors materials. MEDICI simulations have been compared to experimental results characterising the effect of sidewall damage inside the structures made by dry etching.

## Acknowledgements

I would like to acknowledge the TOPS collaboration for providing the laser facility and all the members of the Detector Development group at Glasgow University for assistance in developing the 3D technology. This research was supported by PPARC (UK).

5.45 MeV / 2 scc 2725 keV ~ 500 x 55Fe 458 (916 x if full cts in)

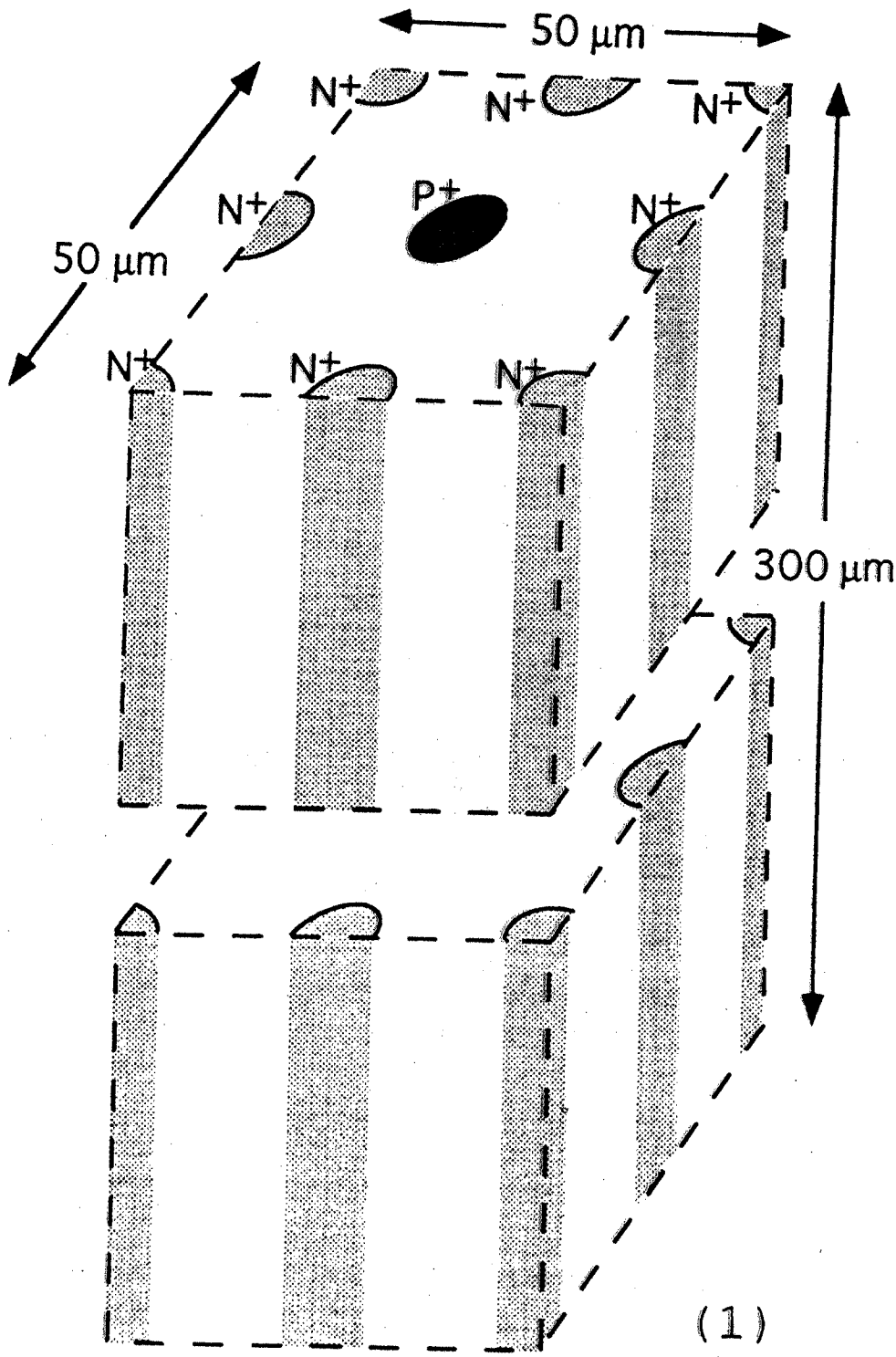



Fig. 1. Three-dimensional view of a typical cell.

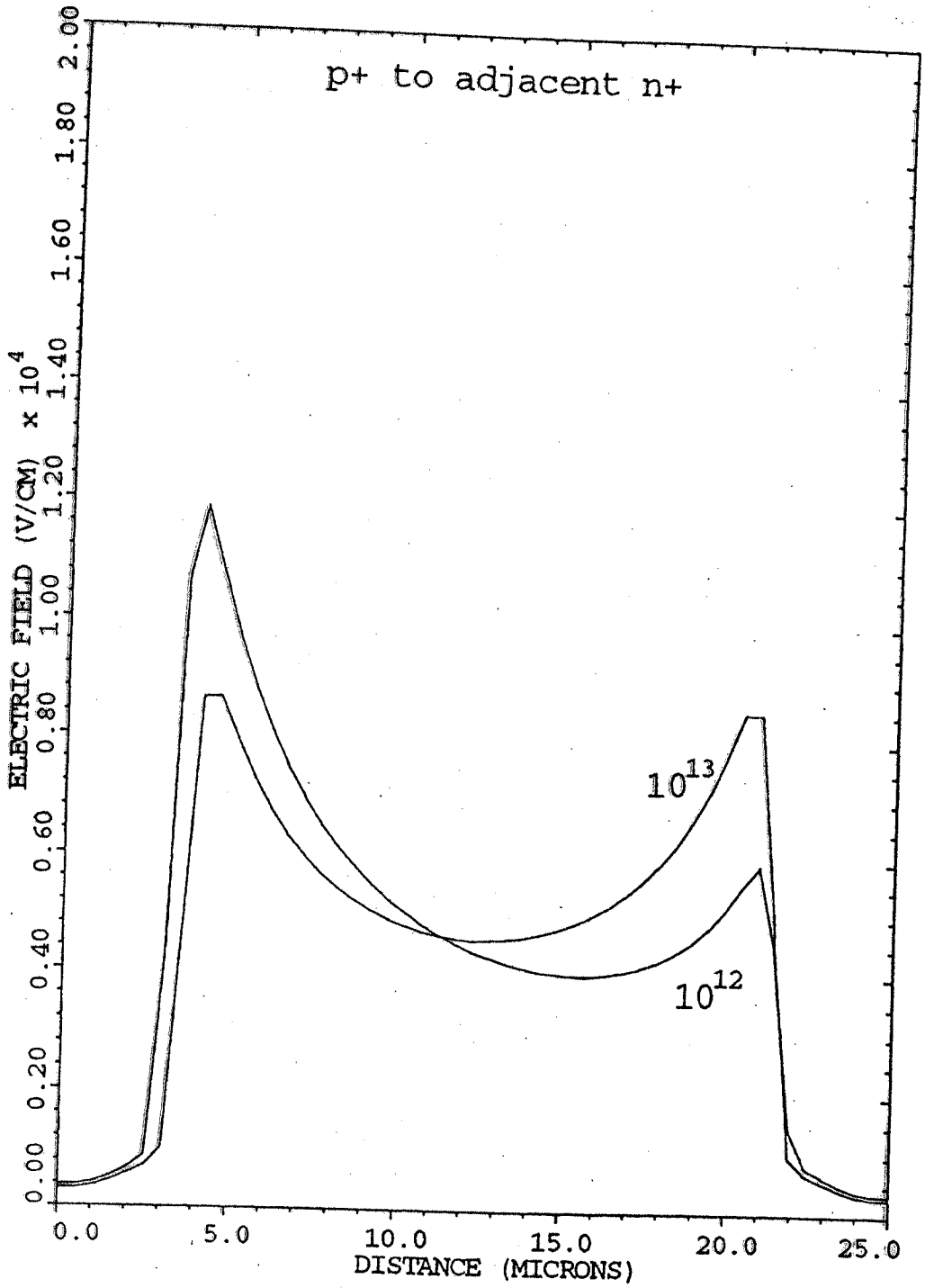



Fig. 5. Comparison of electric field magnitudes for the quarter cell of Fig. 2, 10 V applied voltage, along the line from the $p^+$- to the adjacent $n^+$-electrode for substrate dopings of $10^{12}$/cc and $10^{13}$/cc. With higher substrate dopant levels, as can occur with radiation damage, the peak fields, located where the depletion volume meets the electrodes, actually decrease due to the increase in voltage dropped across the lightly doped (compared to the electrodes) substrate. The small, but non-zero values of the electric fields at the ends of the plot (corresponding to the electrode centers) are due to approximations in the finite-element calculations.

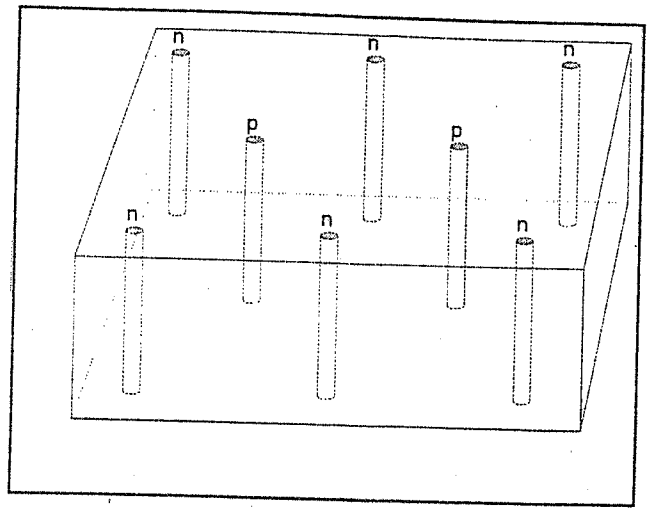



Fig. 1. Three-dimensional view of part of a detector with 3D electrodes penetrating the substrate.

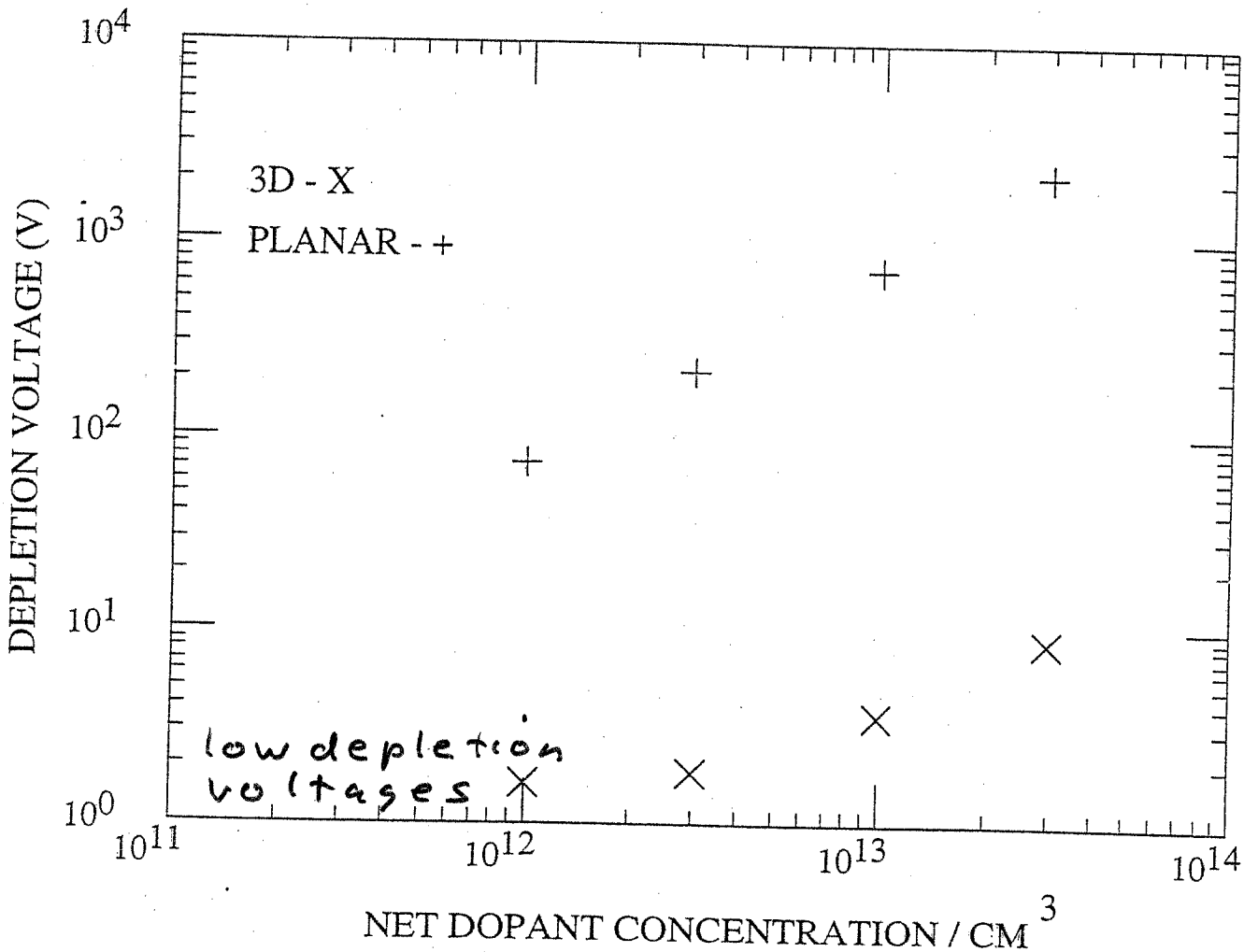
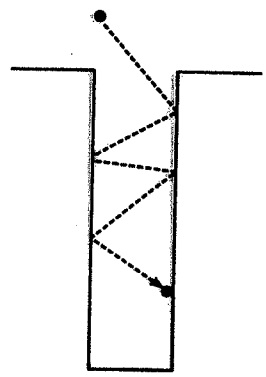



Fig. 2. Calculated depletion voltages for a 300 μm thick, parallel-plate planar diode and for the 3D detector shown at the left with 10 μm diameter electrodes.

# Keys to the technology:

1. Can now etch deep, near-vertical holes. ← teflon
   ↳ (Plasm etch : $SF_6 \rightarrow F_2$ ; Protect sides : $C_4F_8$ →)
2. With low pressure and moderate temperatures, gas molecules used to form polysilicon such as $SiH_4$, $SiH_2Cl_2$, $SiHCl_3$, and $SiCl_4$ will bounce off the hole walls thousands of times before they stick. Mostly they enter, bounce a number of times, and leave. When they stick, it can be anywhere, and so a conformal coat of polysilicon is formed as the H (or Cl) leaves and the silicon migrates to a lattice site.



3. Gasses such as diborane ($B_2H_6$) and phosphine ($PH_3$) can be added to the silane. They also come out in a conformal layer, and make $p^+$ and $n^+$ doped polysilicon.

4. Heating will drive the dopants into the surrounding single crystal silicon, forming the p - n junctions and ohmic contacts in high-quality silicon, keeping electric fields away from the short-lifetime poly.

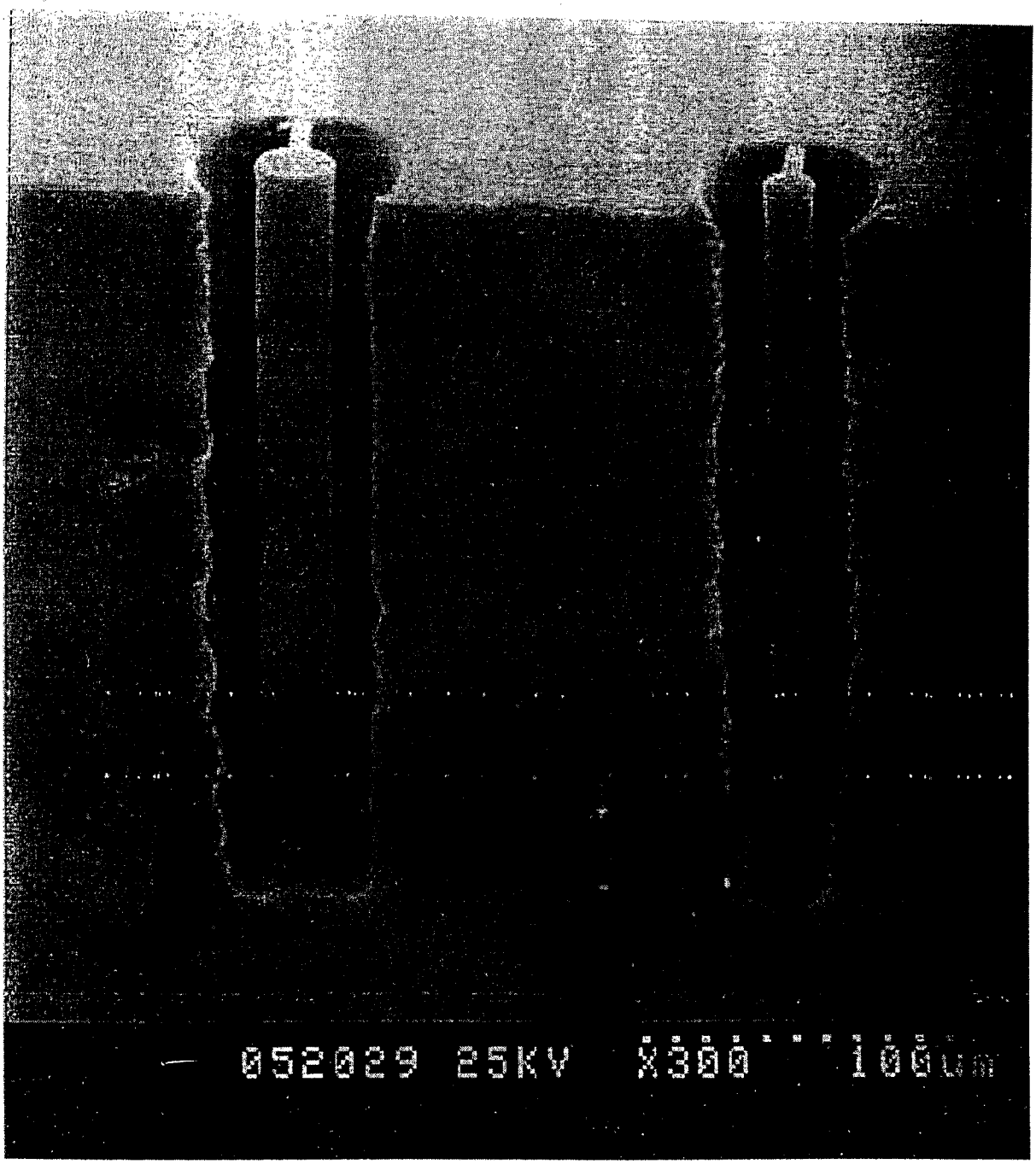



Fig. 1

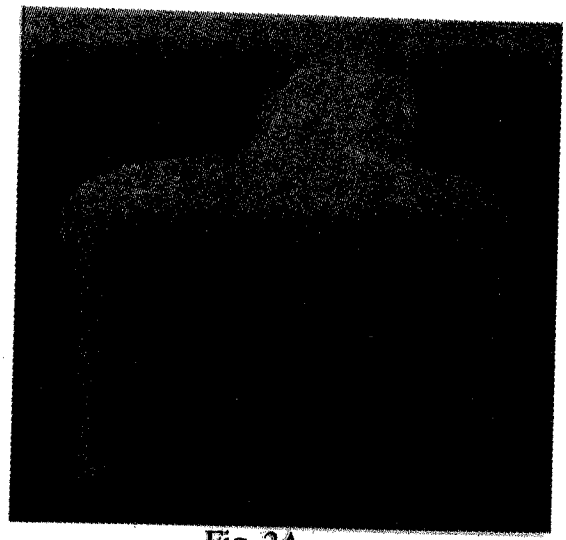


Fig. 2A

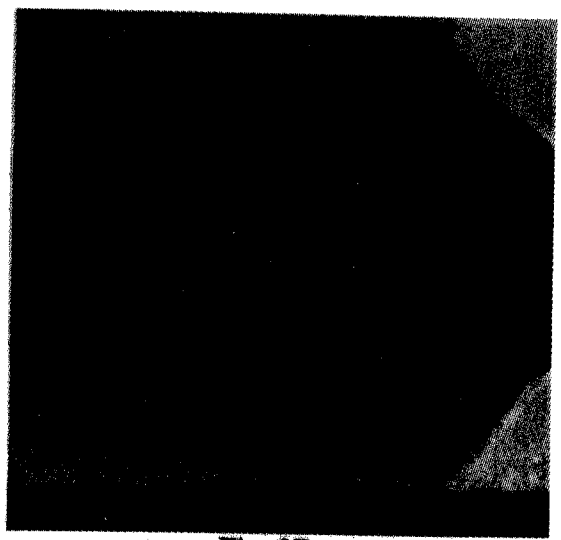


Fig. 2B

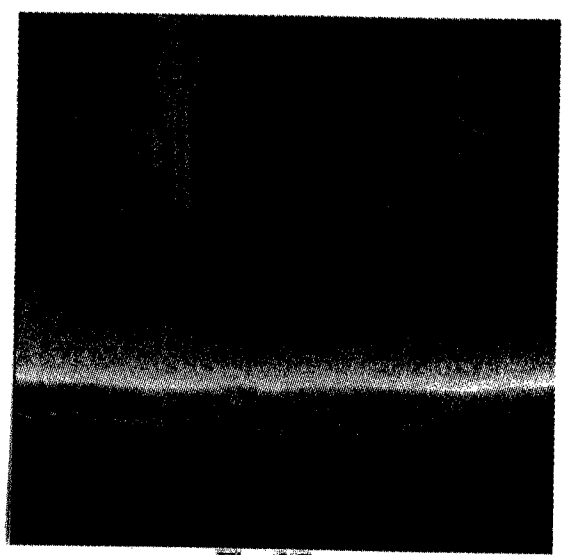
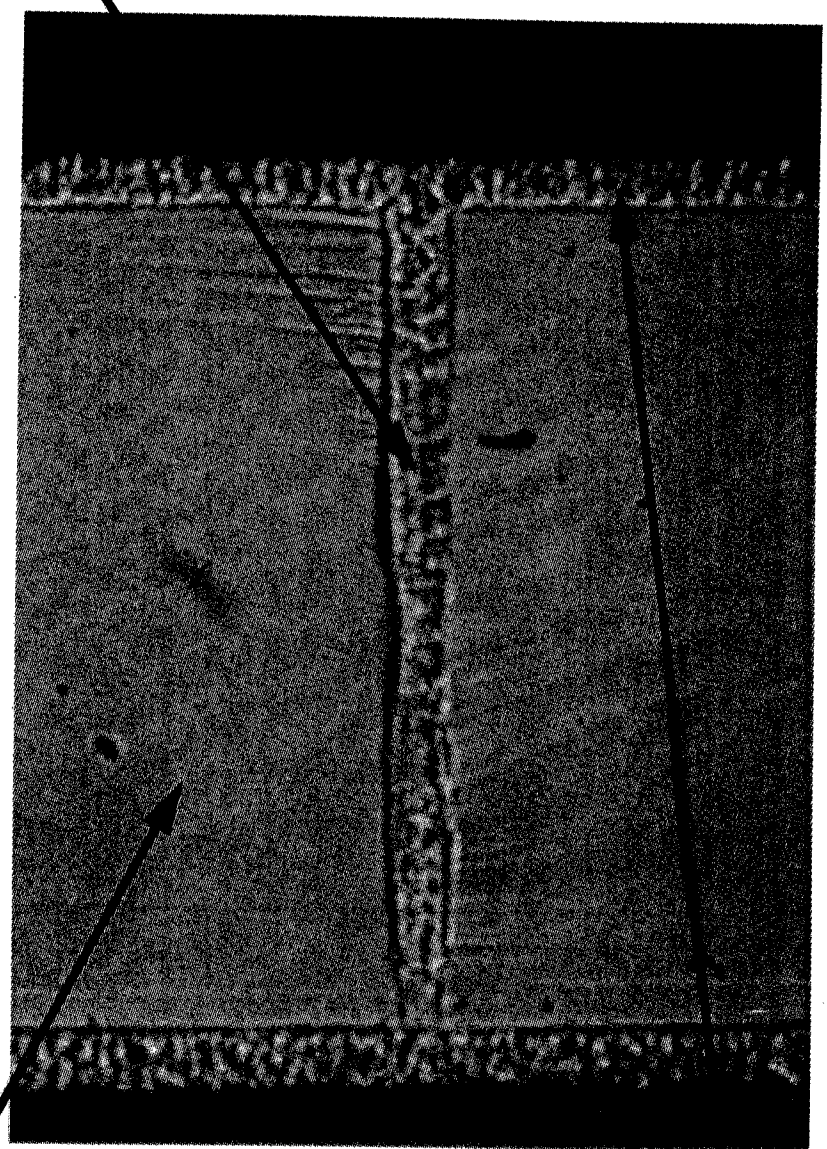
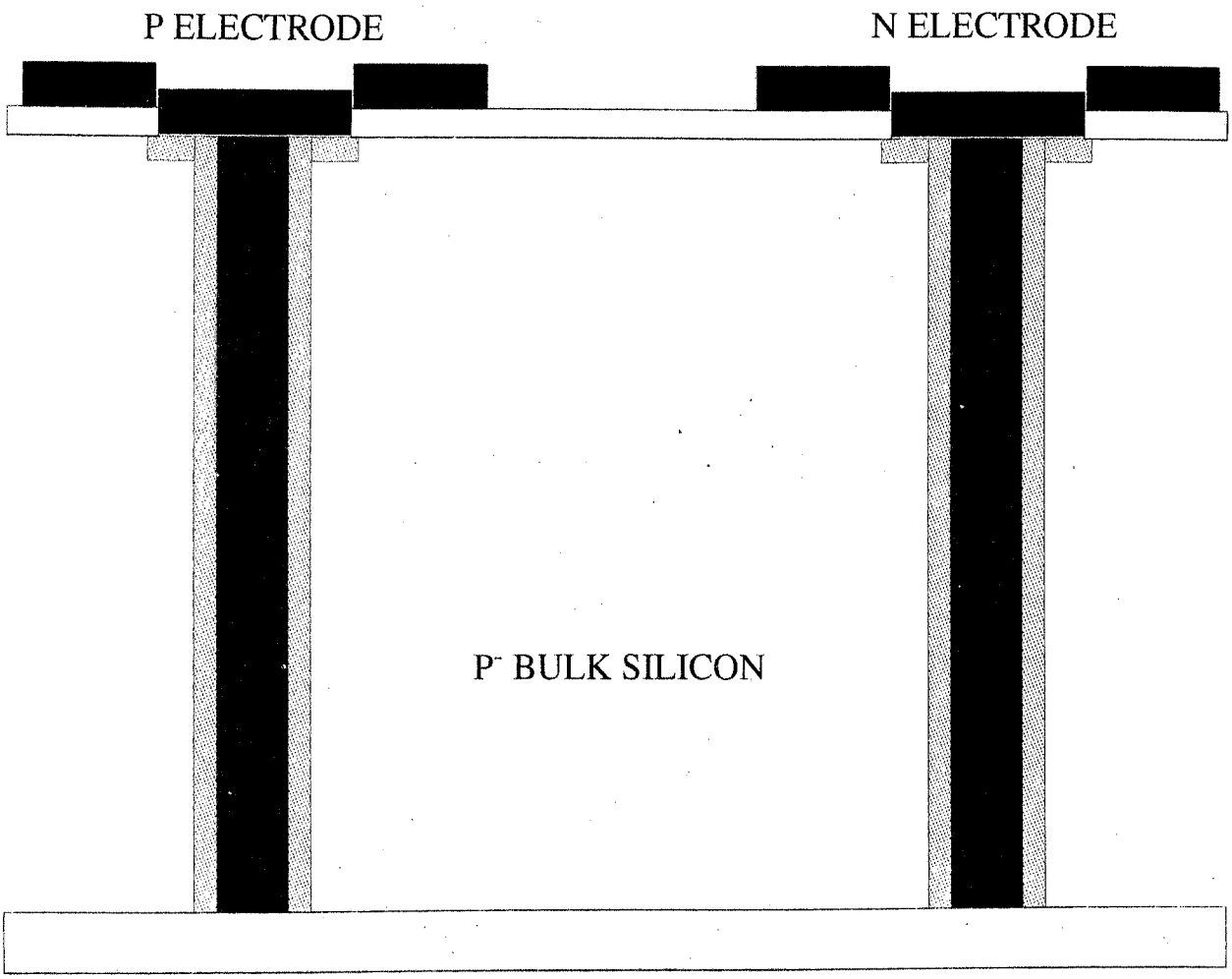


Fig. 2C


ELECTRODE HOLE FILLED WITH POLYSILICON
300-MICRON-THICK
SILICON WAFER
POLYSILICON DEPOSITED
ON TOP AND BOTTOM SURFACES

# DEVICE CROSS SECTION




P-TYPE POLYSILICON

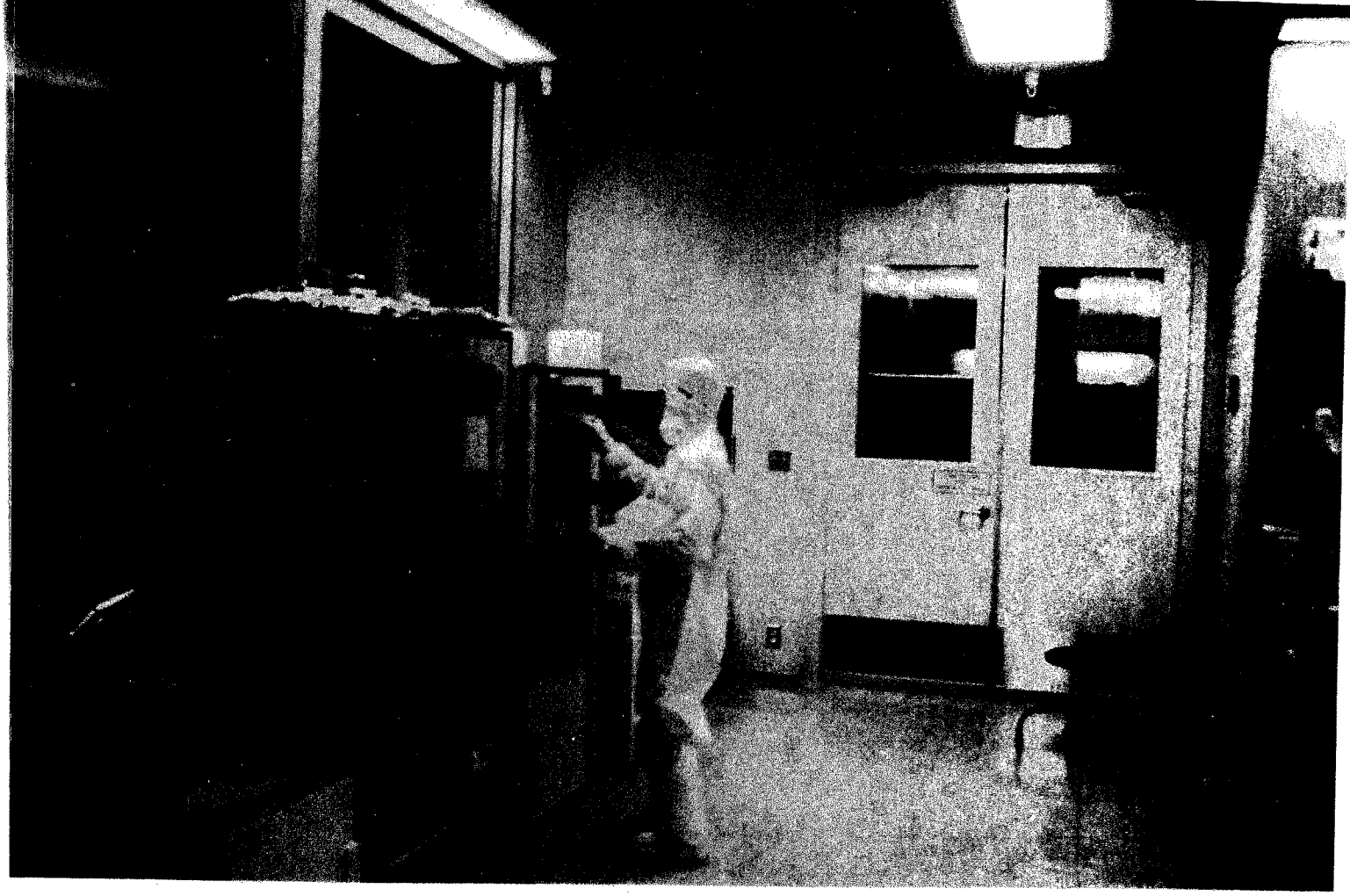
N-TYPE POLYSILICON

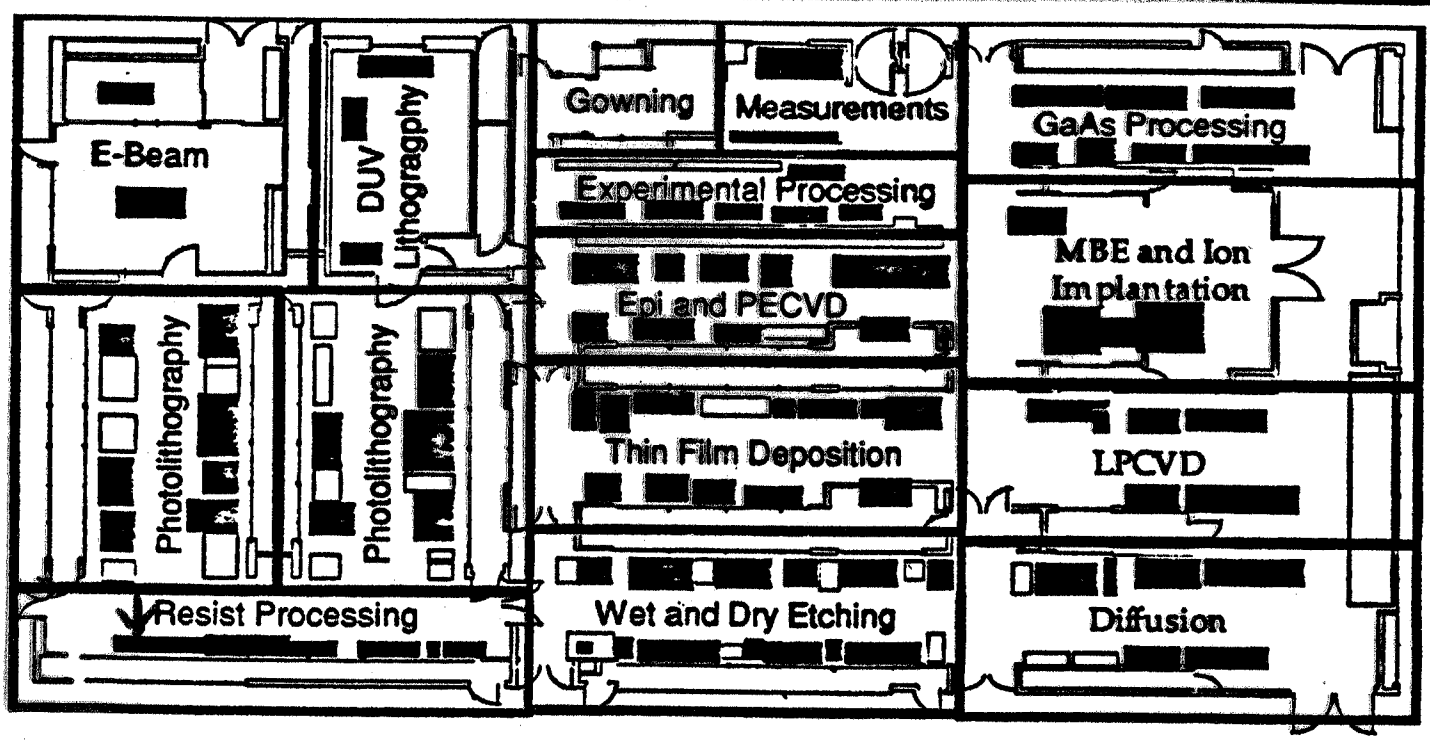
P-TYPE DIFFUSION

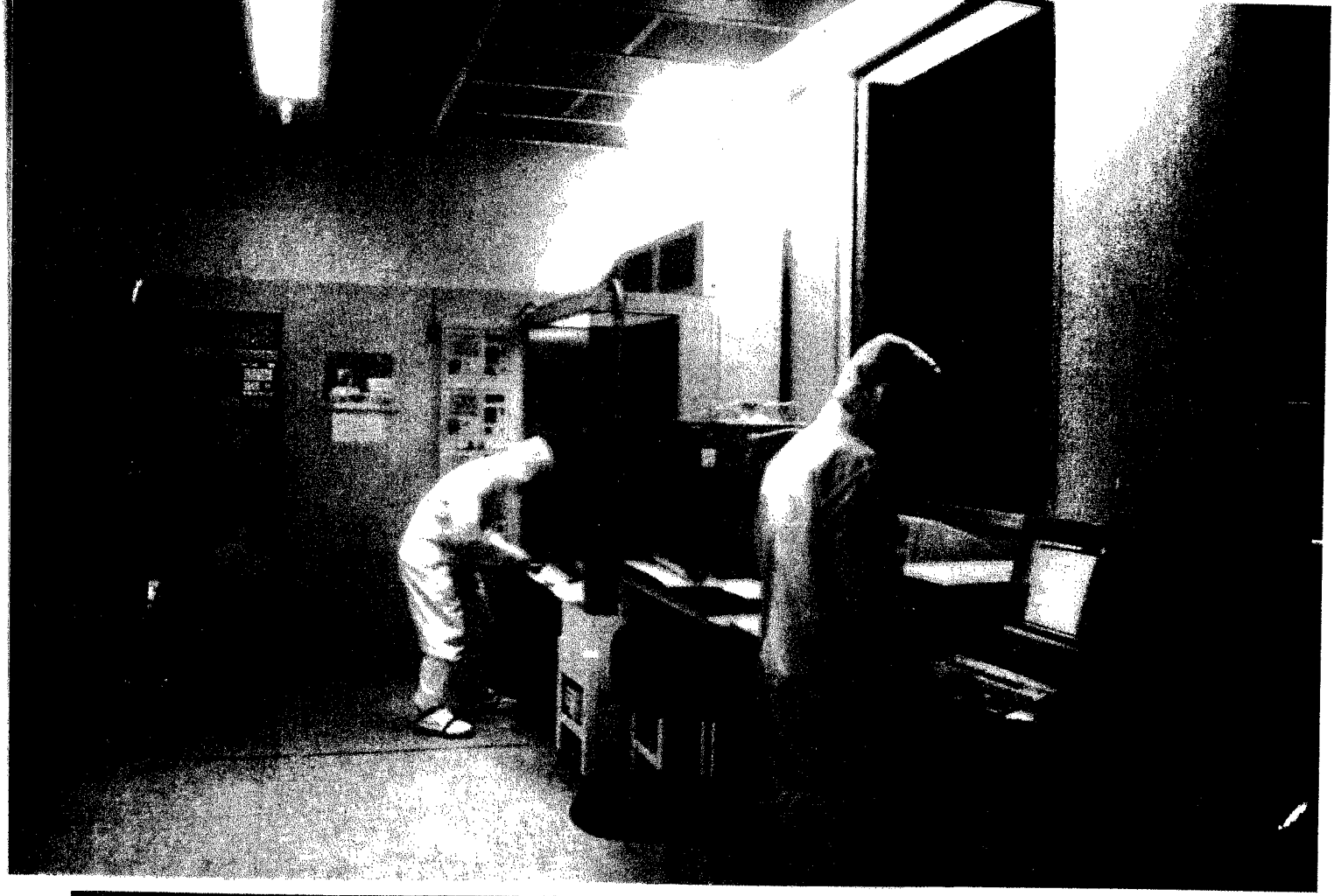
N-TYPE DIFFUSION

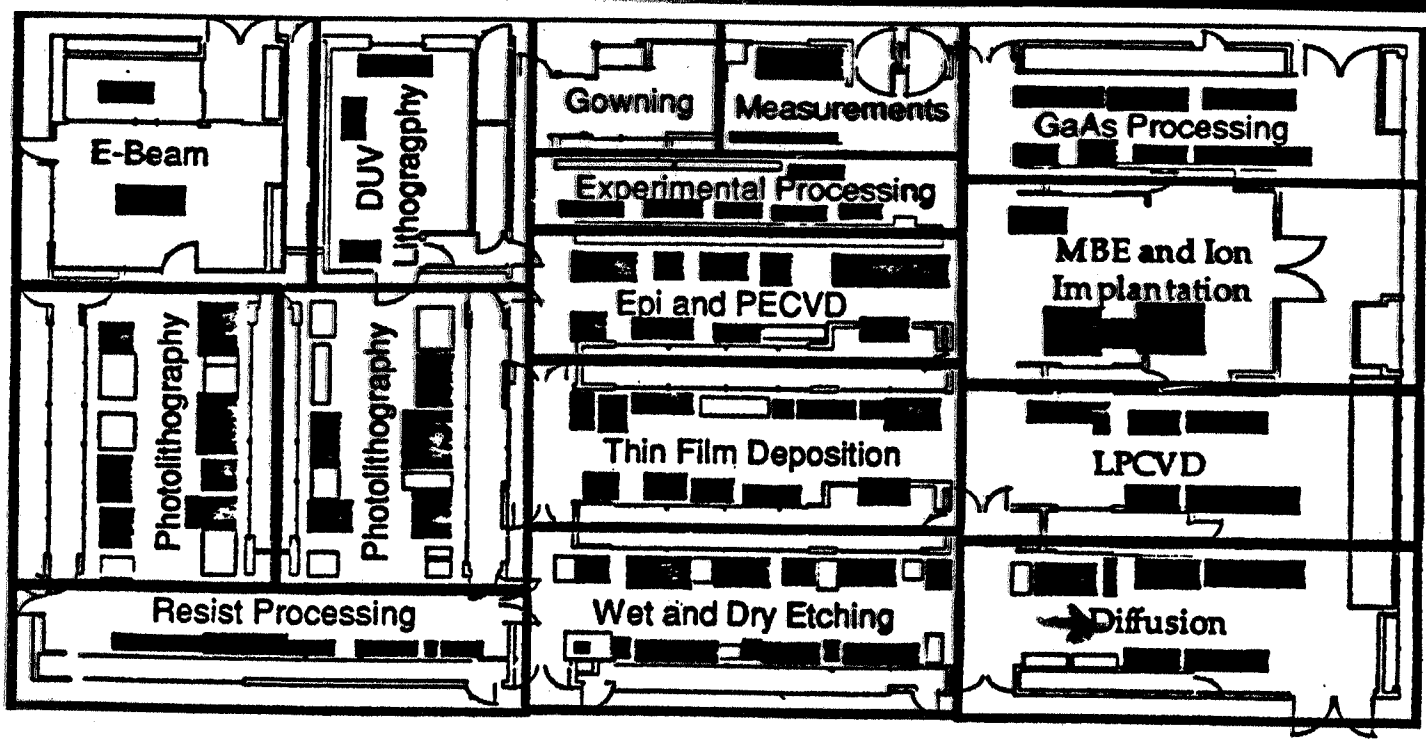
ALUMINUM

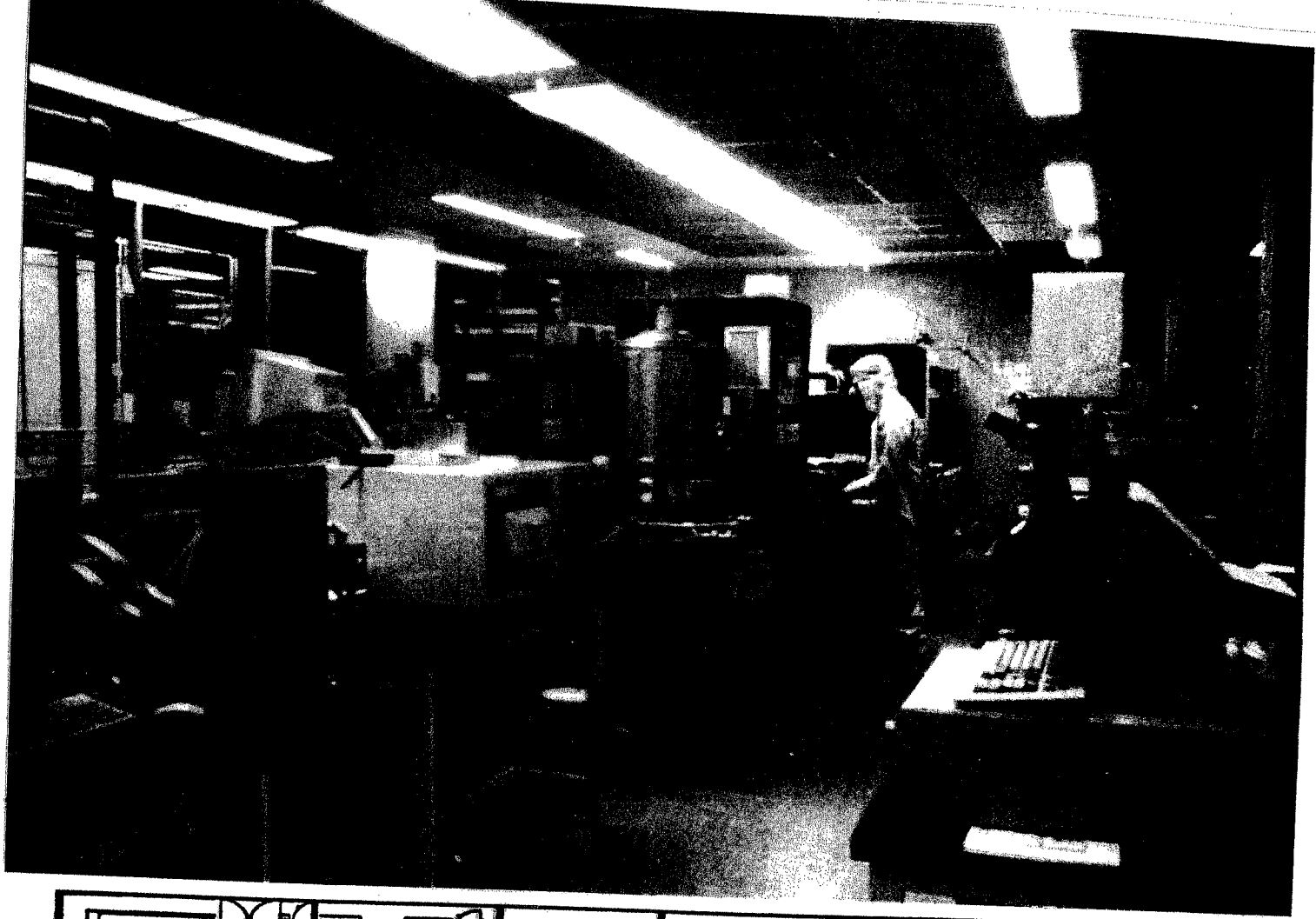
THERMAL OXIDE

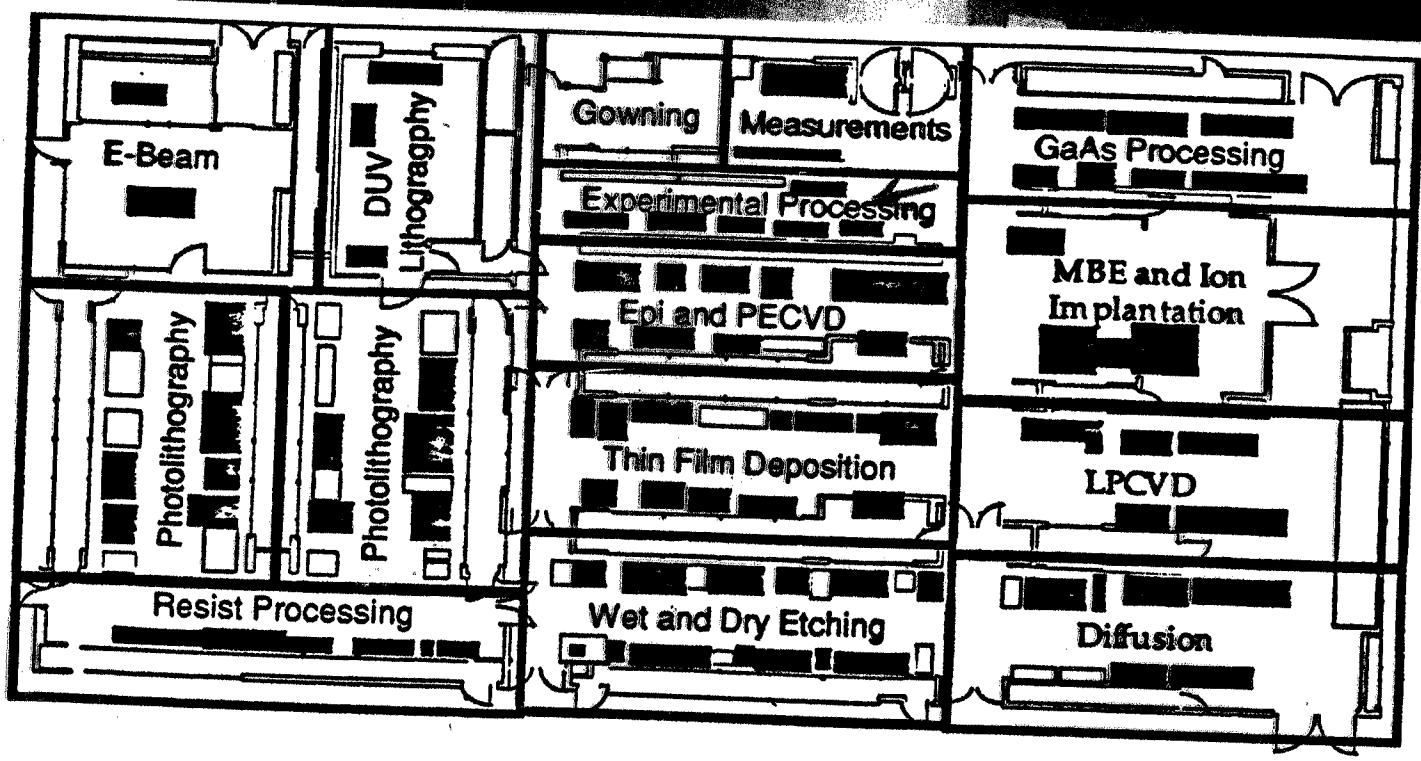



E-Beam
DUV Lithography
Photolithography
Photolithography
Resist Processing
Gowning
Measurements
Experimental Processing
Epi and PECVD
Thin Film Deposition
Wet and Dry Etching
GaAs Processing
MBE and Ion Implantation
LPCVD
Diffusion

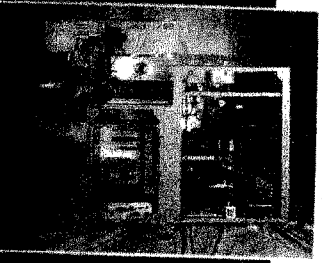



E-Beam
DUV Lithography
Photolithography
Photolithography
Resist Processing
Gowning
Measurements
Experimental Processing
Epi and PECVD
Thin Film Deposition
Wet and Dry Etching
GaAs Processing
MBE and Ion Implantation
LPCVD
Diffusion




E-Beam
DUV Lithography
Photolithography
Photolithography
Resist Processing
Gowning
Measurements
Experimental Processing
Epi and PECVD
Thin Film Deposition
Wet and Dry Etching
GaAs Processing
MBE and Ion Implantation
LPCVD
Diffusion

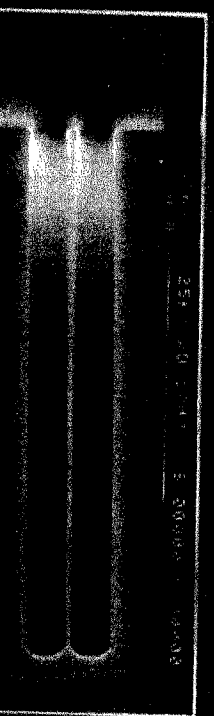
↑
Metallica

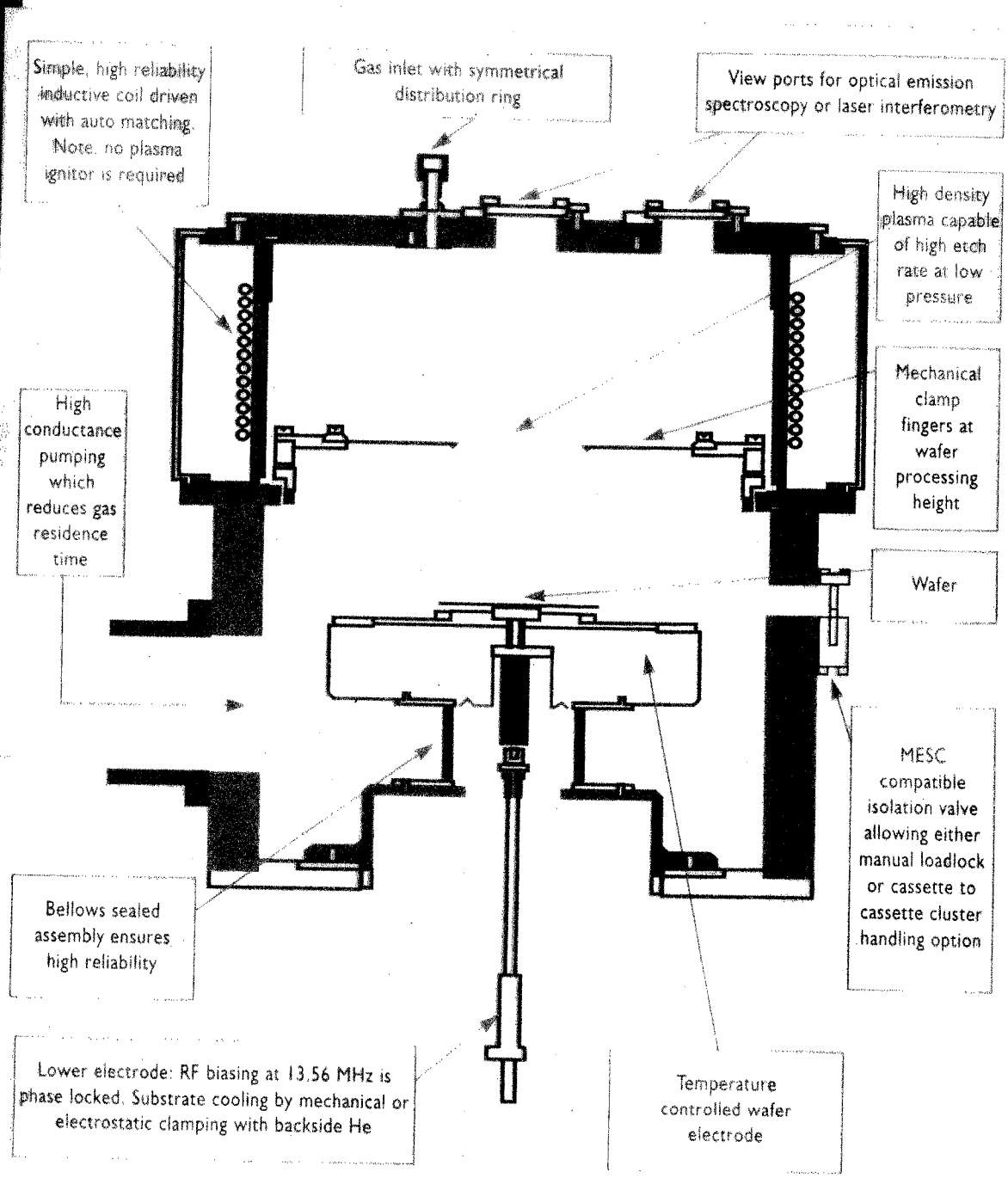


# Multiplex ICP

Conventional plasma sources are unable to meet the progressive demands of modern processes which include higher etch rate and selectivity values, tighter profile control reducing CD and increasing aspect ratio while maintaining minimal microloading and macroloading effects.

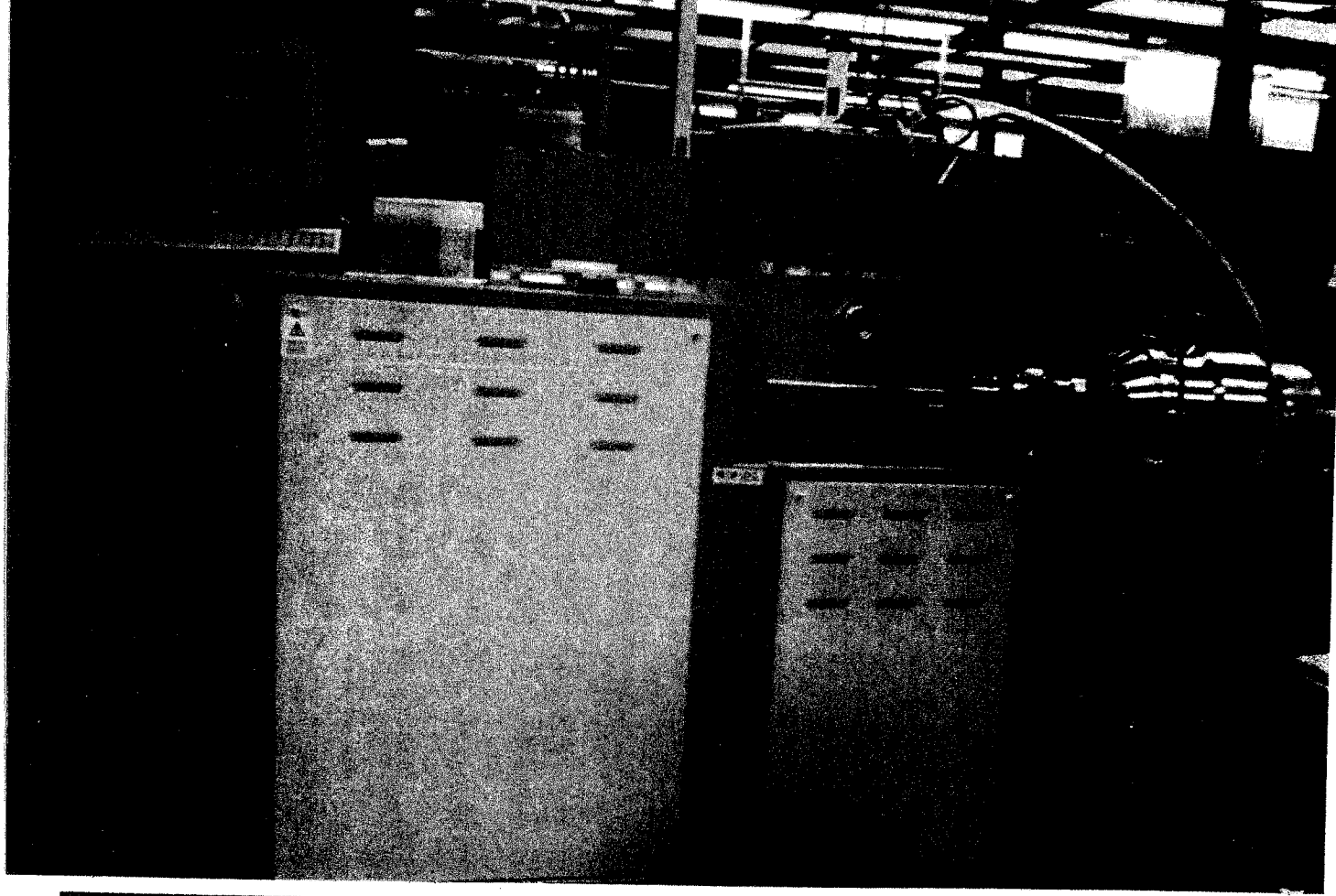
An advancement in plasma source design is essential to accomplish realisation of these requirements. The Multiplex Inductively Coupled Plasma (ICP) from Surface Technology Systems provides the solution.

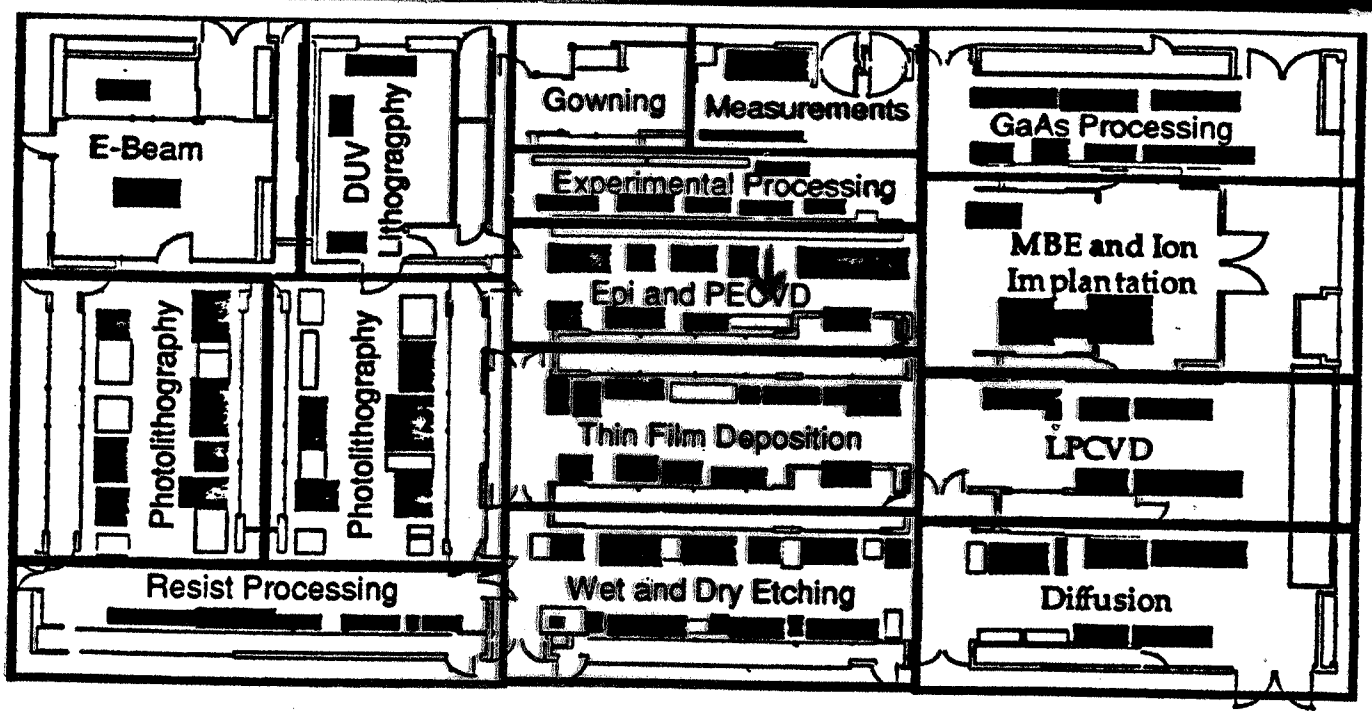


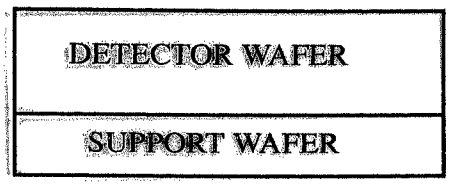



STS

SURFACE TECHNOLOGY SYSTEMS LIMITED PRINCE OF WALES INDUSTRIAL ESTATE ABERCARN NEWPORT GWENT NP1 5AR UK
TELEPHONE +44 (495) 249044 FAX +44 495 249078

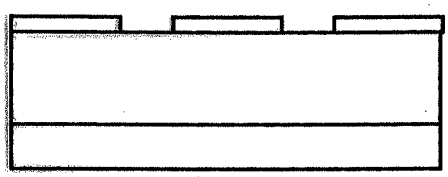



E-Beam
DUV Lithography
Photolithography
Photolithography
Resist Processing
Gowning
Measurements
Experimental Processing
Epi and PECVD
Thin Film Deposition
Wet and Dry Etching
GaAs Processing
MBE and Ion Implantation
LPCVD
Diffusion



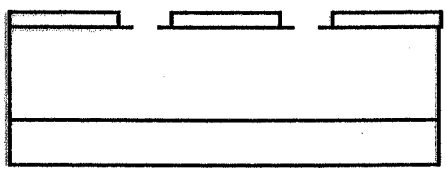

STEPS 1 - 3

OXIDIZE AND FUSION BOND WAFERS



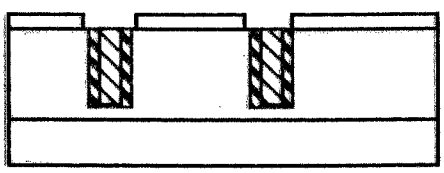
STEPS 4 - 6

PATTERN AND ETCH $P^+$ WINDOW CONTACTS



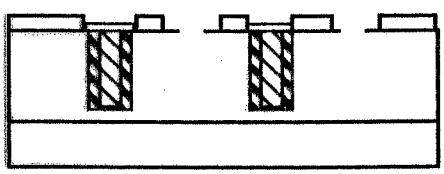
STEPS 7 - 8

ETCH $P^+$ ELECTRODES



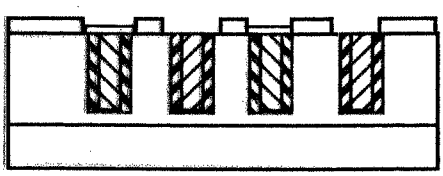
STEPS 9 - 13

DOPE AND FILL $P^+$ ELECTRODES



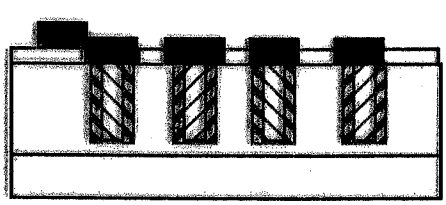
STEPS 14 - 17

ETCH $N^+$ WINDOW CONTACTS AND ELECTRODES



STEPS 18 - 23

DOPE AND FILL $N^+$ ELECTRODES



STEPS 24 - 25

DEPOSIT AND PATTERN ALUMINUM

| Step | Mask | Clean | Purpose | Parameters |
|---|---|---|---|---|
| 1 | | 1,2 | oxidize detector, support wafers | 0.8 micron, 1100 C, wet oxide |
| 2 | | 6 | bond detector, support wafers | align, contact, anneal at 1100 C |
| 3 | | | thin and polish detector wafer | done by outside firm |
| 4 | 1 | 1 | etch alignment marks | silicon plasma etch, $C_2ClF_5$ |
| 5 | | 1,2 | field oxide | 0.7 micron, 1000 C, wet oxide |
| 6 | 2 | | etch n-type contact windows | buffered $HF/H_2O$ (1/6) |
| 7 | 3 | 1 | n-type electrodes | 7.0 micron thick resist |
| 8 | | | etch deep n column holes | high-aspect etch using STS |
| 9 | | 4,1,2 | deposit poly getter/electrode layer | $SiH_4$ source, 620 C, 0.46 Torr |
| 10 | | 2* | phosphorus doping of poly | $POCl_3$ source, 30 min., 950 C |
| 11 | | 2* | drive phosphorus into silicon | 1 hour, 1000 C in nitrogen |
| 12 | | 5,2* | fill holes with more poly | $SiH_4$ source, 620 C, 0.46 Torr |
| 13 | | | remove poly from both wafer surfaces | silicon plasma etch, $C_2ClF_5$ |
| 14 | | 2 | grow oxide for n-column caps | 0.2 micron, 1000 C, wet oxide |
| 15 | 4 | 1 | etch p-type contact windows | buffered $HF/H_2O$ (1/6) |
| 16 | 5 | 1 | p-electrodes | 7.0 micron thick resist |
| 17 | | 1,2,4 | etch deep p column holes | high-aspect etch using STS |
| 18 | | 1,2,4 | deposit poly getter/electrode layer | $SiH_4$ source, 620 C, 0.46 Torr |
| 19 | | 2* | boron doping of poly | $BBr_3$ source, 30 min., 955 C |
| 20 | | 2* | drive boron into silicon | 1 hour, 1000 C in nitrogen |
| 21 | | 5, 2* | fill holes with more poly | $SiH_4$ source, 620 C, 0.46 Torr |
| 22 | | | remove poly from both wafer surfaces | silicon plasma etch, $C_2ClF_5$ |
| 23 | | | remove barrier oxide | buffered HF acid etch |
| 24 | 6 | 5 | Al metal deposition and pattern | 1.0 micron Al/Silicon (99/1) |
| 25 | | 3 | forming gas anneal | 45 min., 400 C, hydrogen |

Table 1a -- Fabrication Steps

Cleaning steps indicated in the third column are completed before the rest of the step. Cleaning steps 2* may be omitted if the step immediately follows the preceding step. The specific cleaning steps are:

1: 20 min $H_2SO_4/H_2O_2$ (4/1)-120 C, dump rinse, spin rinse
2: 10 min $H_2SO_4/H_2O_2$ (4/1)-90 C, dump rinse, 10 min $HCl/H_2O_2/H_2O$ (1/1/5)-70 C dump rinse, spin rinse, dry
3: 20 min EMT-130T-90 C; dump rinse, spin rinse, 5 min PRS-1000-40 C, dump rinse, spin rinse
4: 5 min in oxygen plasma
5: 2 min $HF/H_2O$ (1/20)
6: 10 min $H_2SO_4/H_2O_2$ (4/1)-90 C,, dump rinse, spin rinse

**Items omitted from initial (2 month) fabrication run:**

**(to determine, quickly, if the technology would work)**

1. **simulations for fabricated geometries, including surface effects (only Bari paper geometries simulated)**
2. **optimization of STS etching parameters for small d / l**
3. **field implants**
4. **guard rings around electrodes**

   **(requires double-sided processing and ~~may~~ is not ~~be~~ needed, but might provide useful information on leakage currents)**

5. **active edges** - but we have results from trench electrodes
6. **only one thickness fabricated (121 microns)**

# WHAT's ON THE WAFER

(partial list)

## Fabrication Test Structures

Variable Width Cylinder and Trench Array

Implant/Metal Contact and Resistance Structures

Through-wafer Conduction Vias

Polysilicon Growth and Resistance Structures

## C-V and I-V Measurement Structures

Parallel Plates

Concentric Cylinders

Ganged Offset Row Strip Arrays (7 designs)

## Detectors

Offset Row Strips - 100 micron pitch, 1 millimeter long, 14 micron holes (on mask)
(4 designs)

Offset Row Strips - 100 micron pitch, 1 centimeter long

Offset Row Strips - 100 micron pitch, 1 millimeter long, 6 micron holes (on mask)

Offset Row Pixel Array - All P Electrodes Go To Wire Bond Pads
(4 designs)

Offset Row Strips - Some Isolated Electrodes Go To Probe Pads
(2 designs)

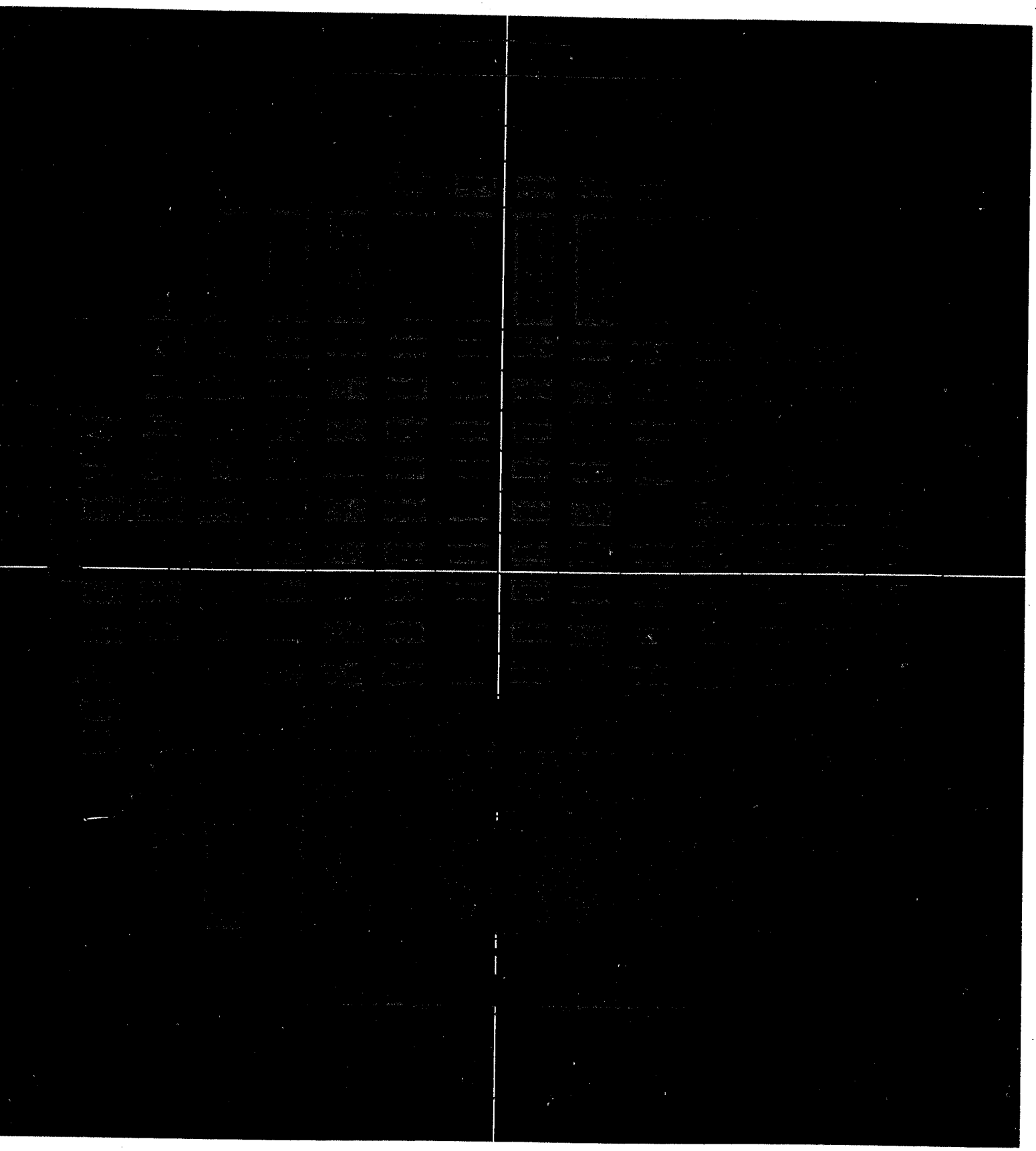
Cylinder-Plate Arrays

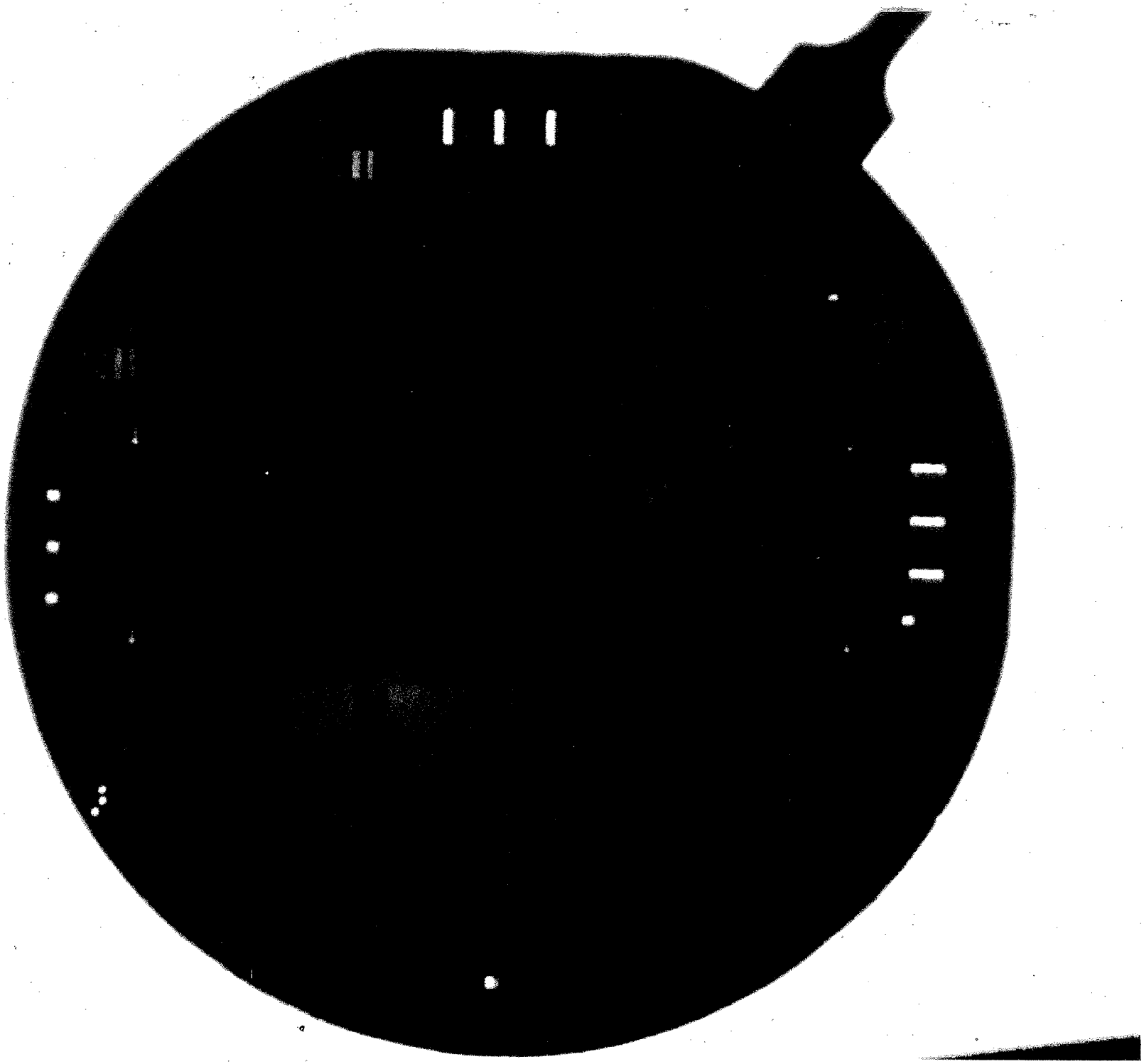
Hexagonal Arrays

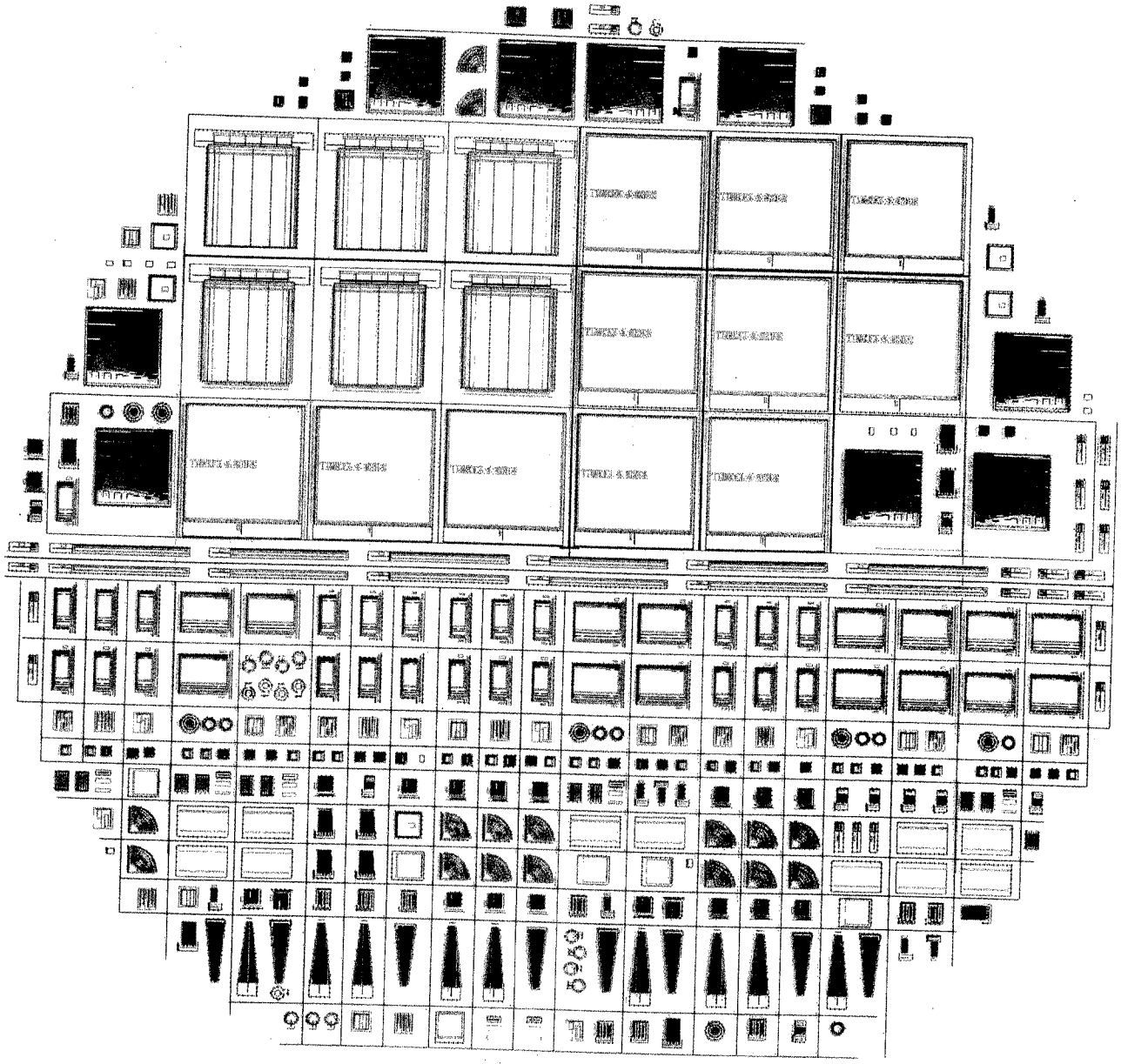
ATLAS Pixel Detector - All P Electrodes to Bumps, N electrodes to probe pads
(2, 3 electrodes/bump; ganged structures for electrical tests) (5)

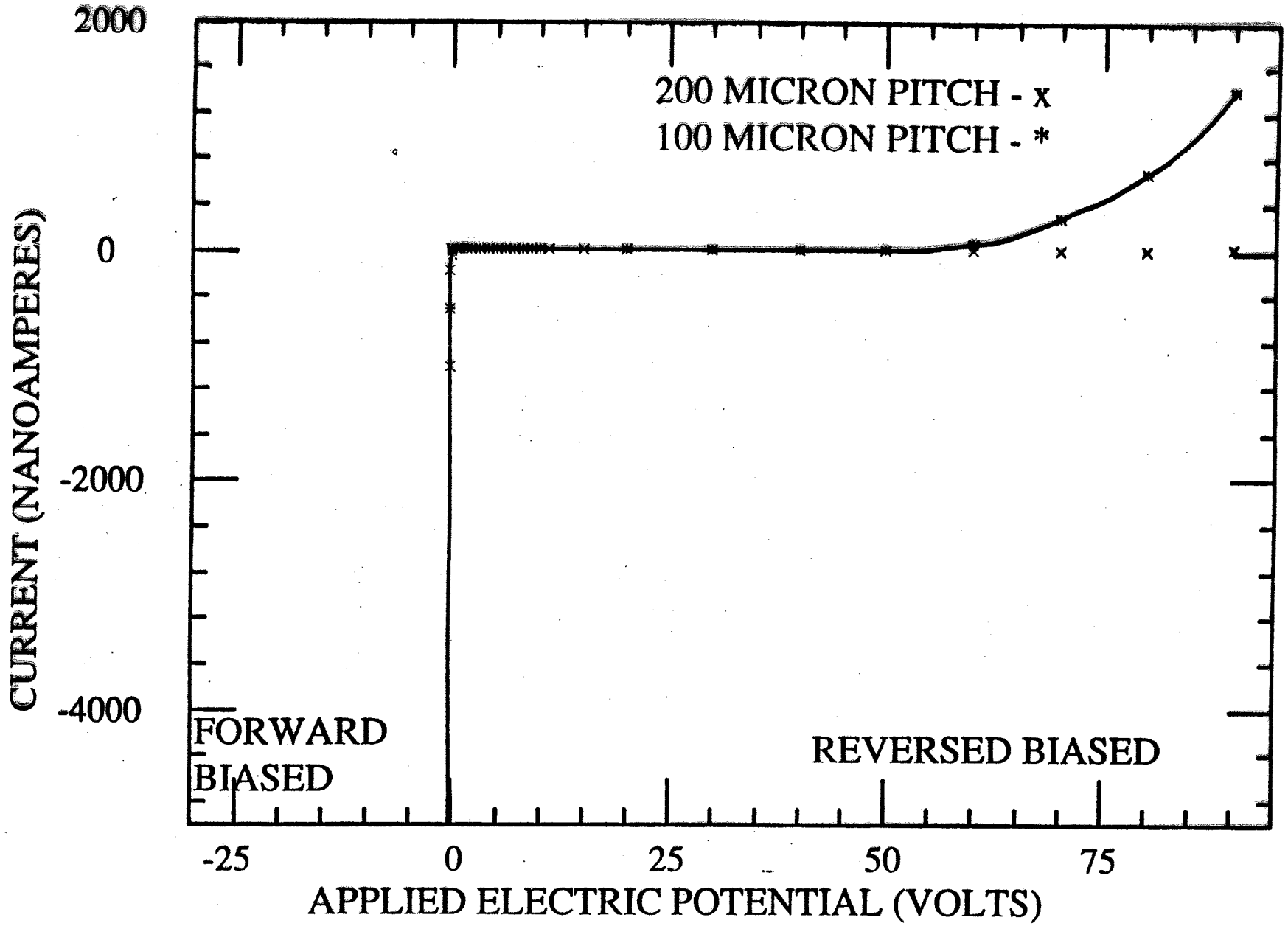
active edge test structures
(6 designs: 1, 2, 3 active edges – n doped edges
oxide edges)

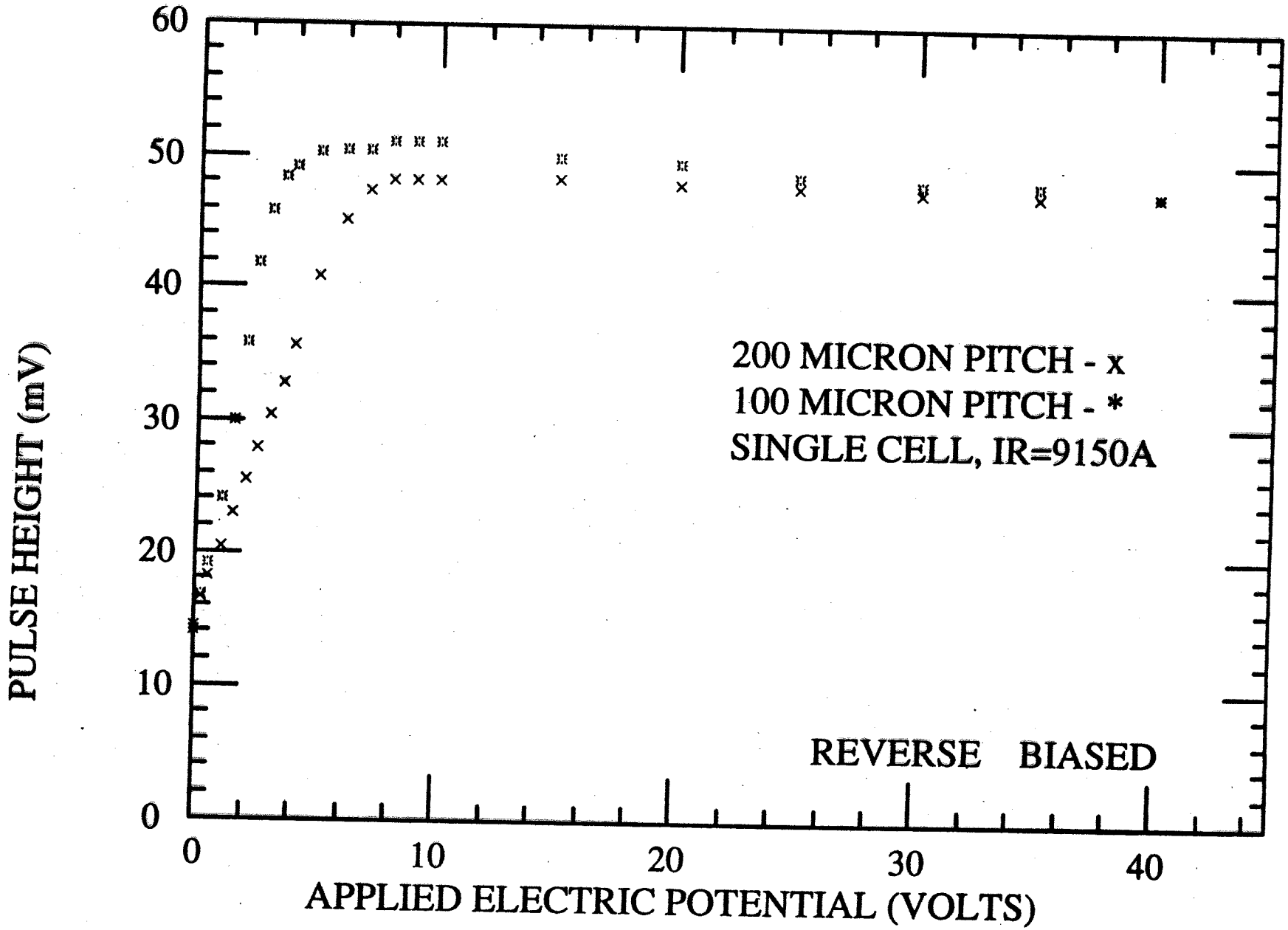
vernier alignment checker, exposure checking targets, ...








2000
0
-2000
-4000
CURRENT (NANOAMPERES)
200 MICRON PITCH - x
100 MICRON PITCH - *
FORWARD
BIASED
REVERSED BIASED
-25
0
25
50
75
APPLIED ELECTRIC POTENTIAL (VOLTS)


60
50
40
30
20
10
0
PULSE HEIGHT (mV)
200 MICRON PITCH - x
100 MICRON PITCH - *
SINGLE CELL, IR=9150A
REVERSE BIASED
0
10
20
30
40
APPLIED ELECTRIC POTENTIAL (VOLTS)

# TESTS WITH GAMMA AND X-RAY SOURCES

C. Kenney, S. Parker, B. Krieger, B. Ludewigt

PERFORMED AT LAWRENCE BERKELEY NATIONAL LABORATORY

CHARGE-SENSITIVE, 16-CHANNEL PREAMPLIFIER
(Ludewigt, et al., IEEE Trans. Nucl. Sci., vol. 41, No. 4, (1994) pp. 1037-1041)

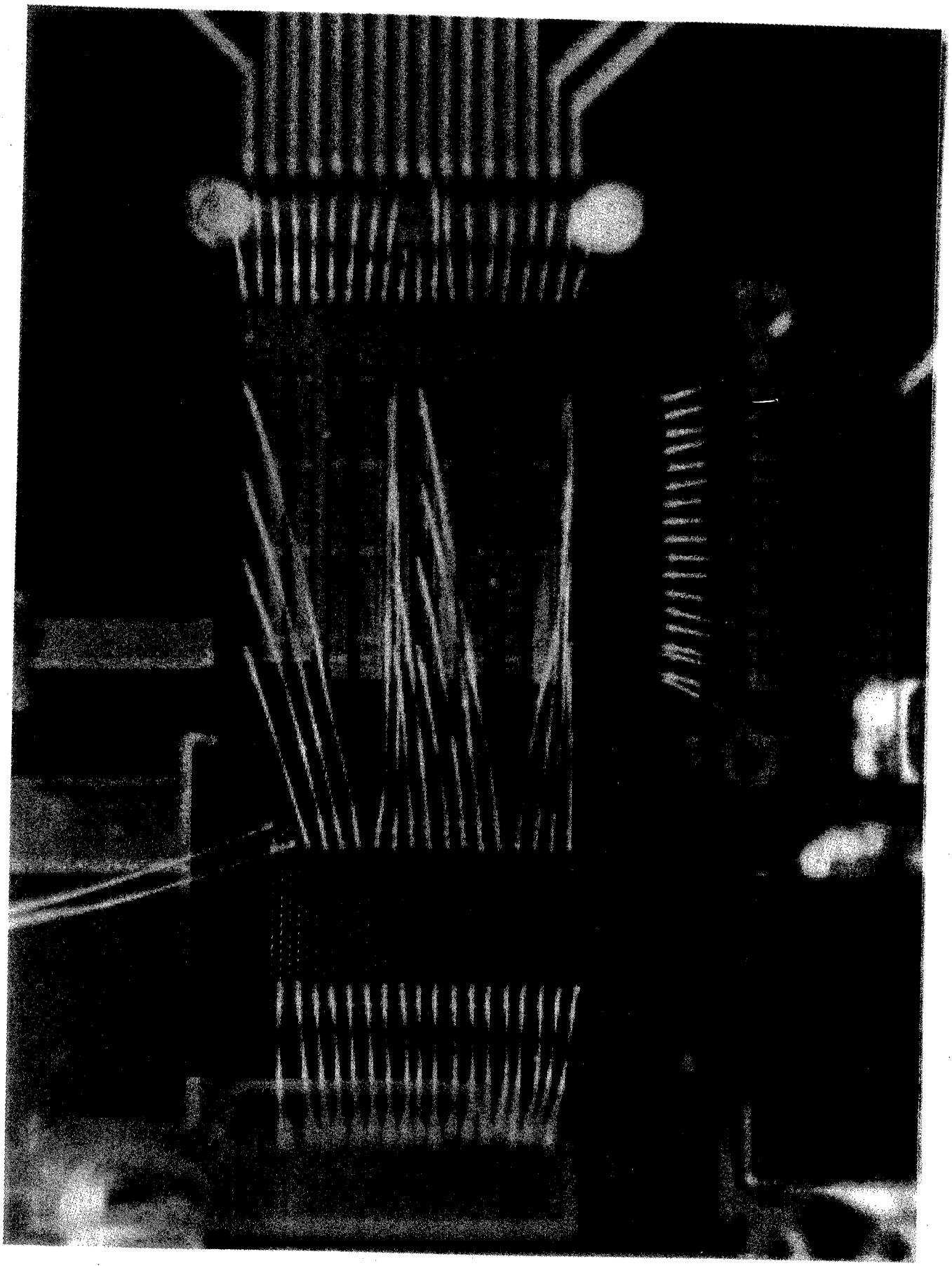
ROOM TEMPERATURE

SHAPING TIME OF 1 MICROSECOND

USED A STRIP DETECTOR WITH 14 P-TYPE ELECTRODES TIED TOGETHER WITH ALUMINUM

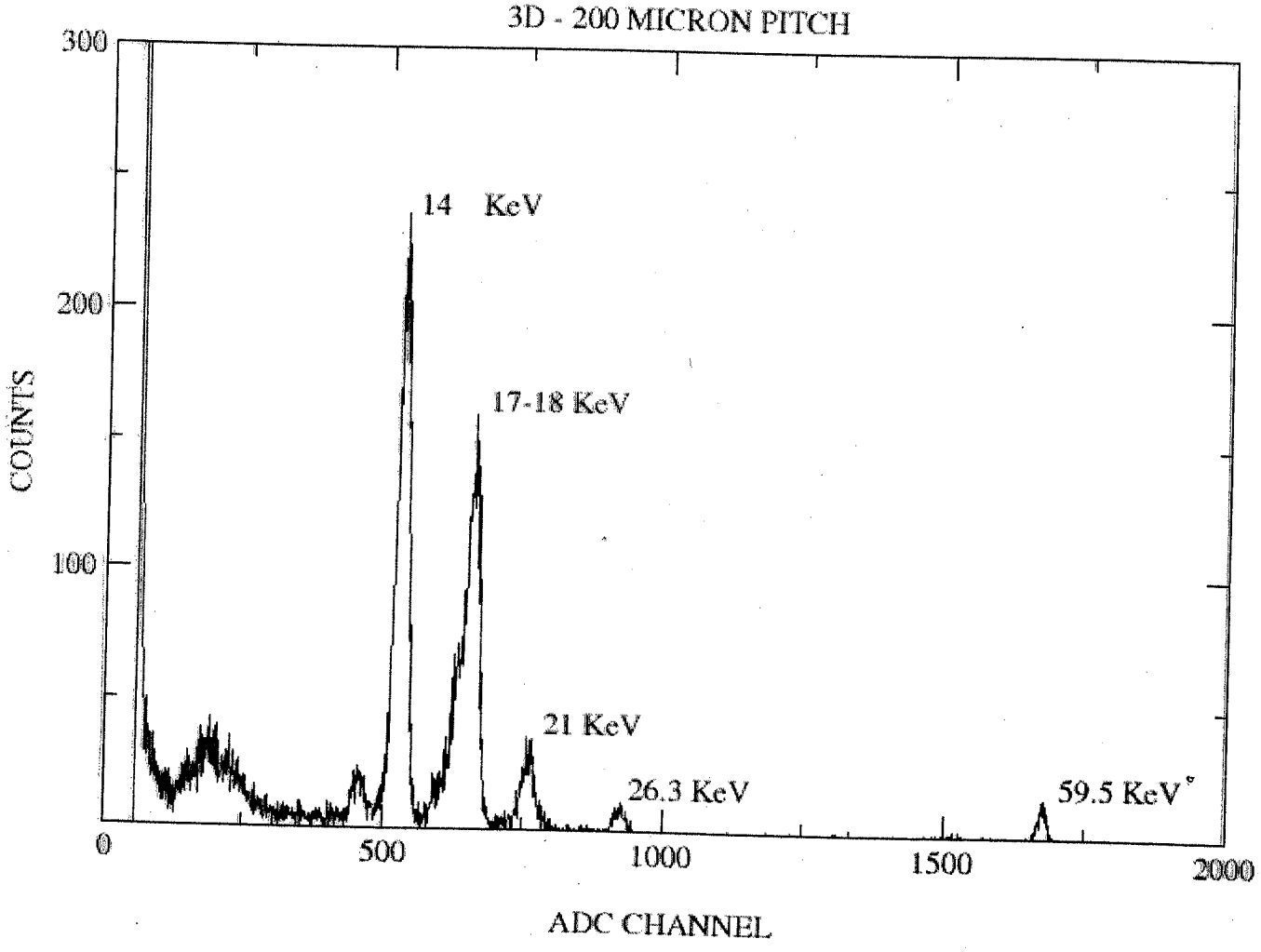
200-MICRON PITCH P STRIP TO P STRIP

100-MICRONS BETWEEN P ELECTRODES WITHIN A STRIP

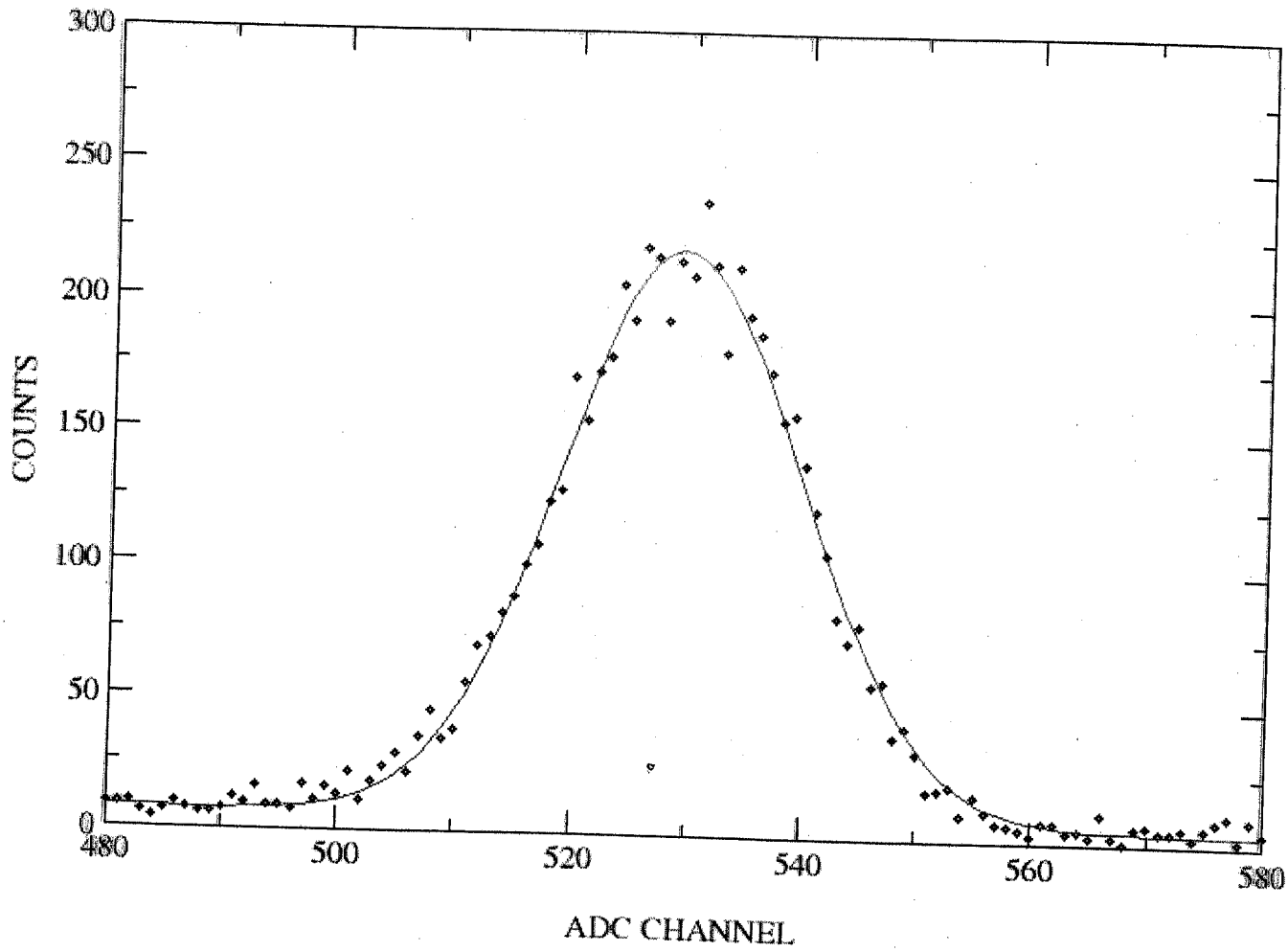


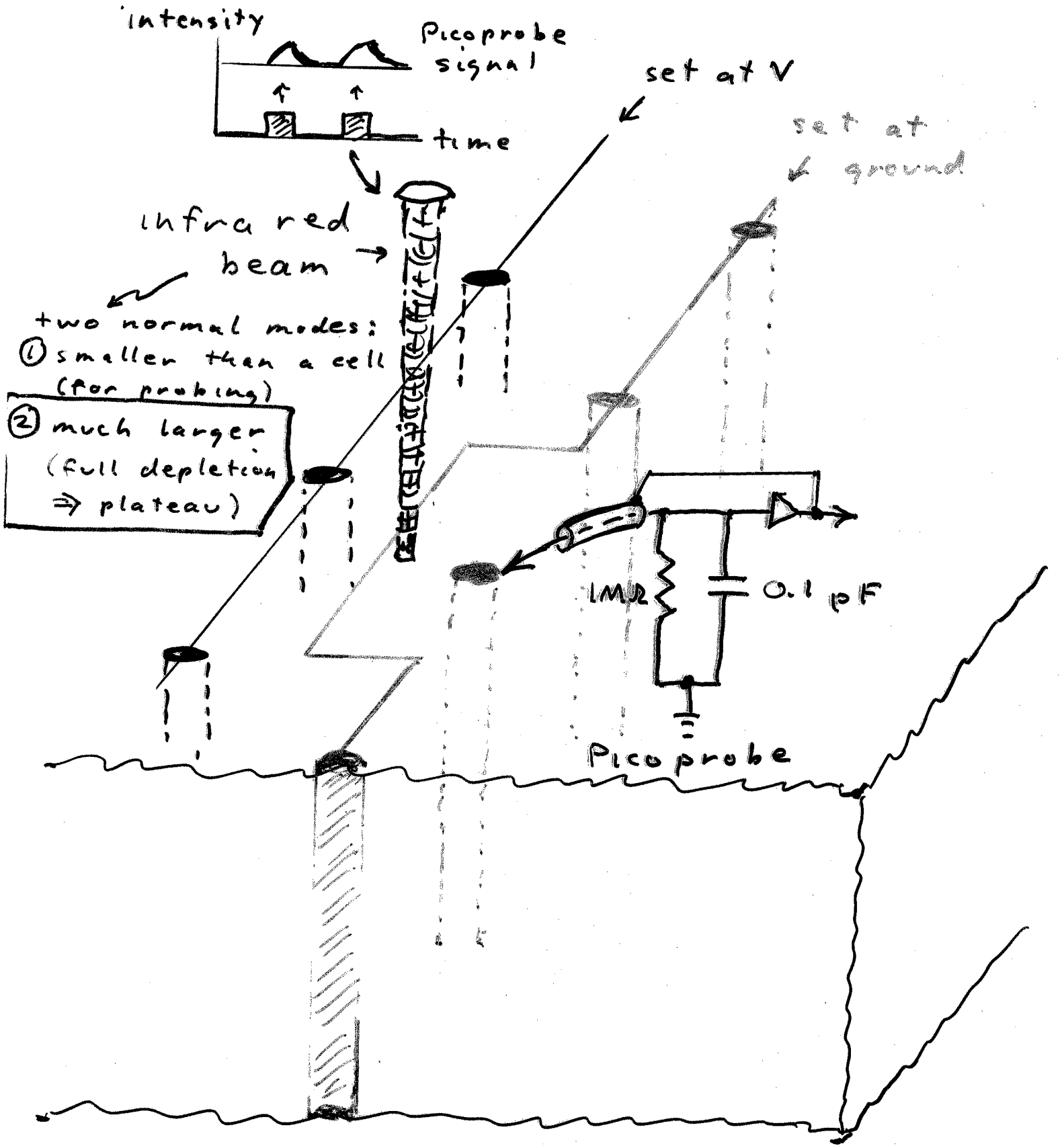
# AMERICIUM-241

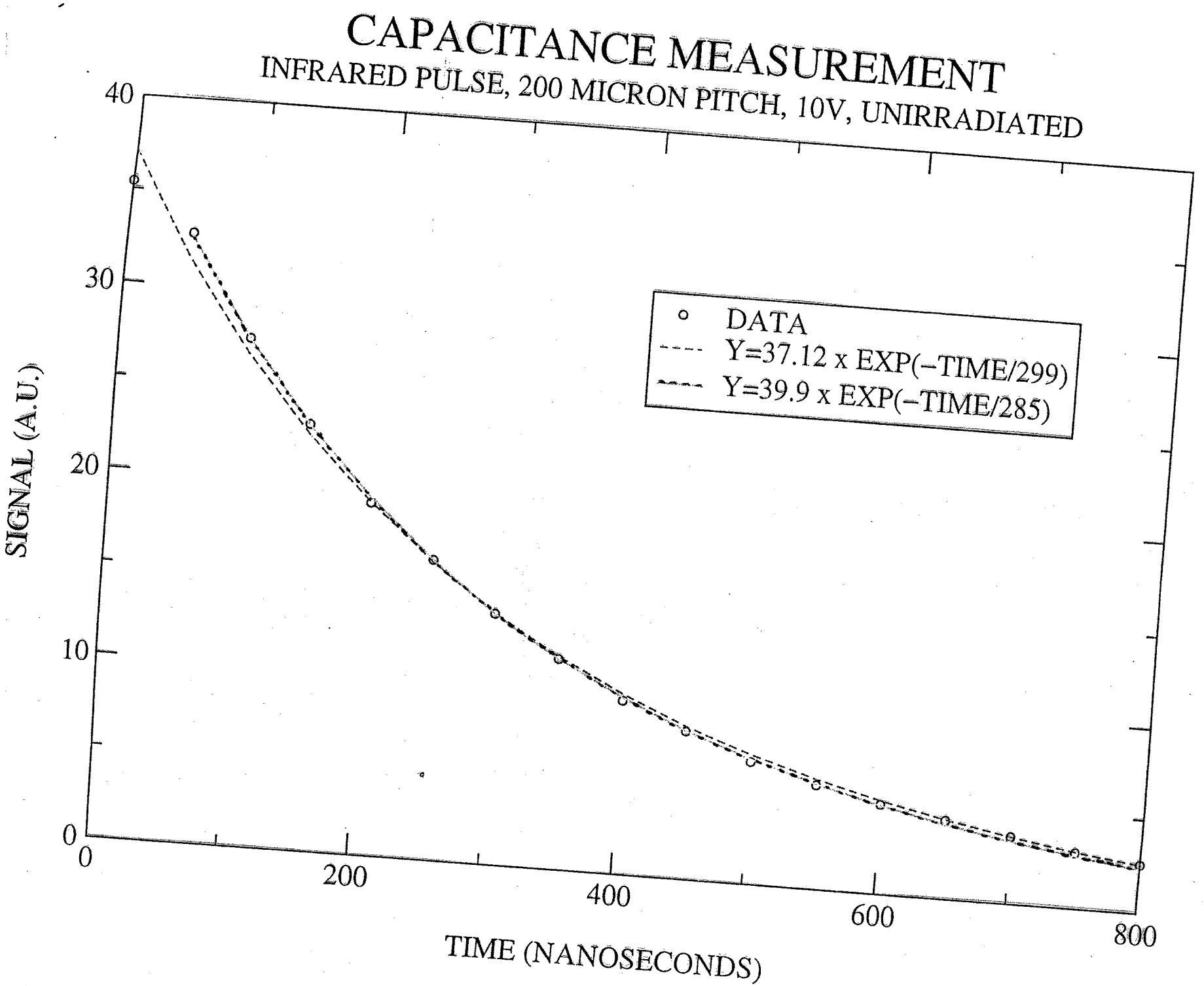
3D - 200 MICRON PITCH



# AMERICIUM 14 KeV PEAK




intensity
Picoprobe signal
time
set at V
set at ground
infrared beam
two normal modes:
① smaller than a cell (for probing)
② much larger (full depletion ⇒ plateau)
1MΩ
0.1 pF
Picoprobe


CAPACITANCE MEASUREMENT
INFRARED PULSE, 200 MICRON PITCH, 10V, UNIRRADIATED
SIGNAL (A.U.)
TIME (NANOSECONDS)
0
10
20
30
40
0
200
400
600
800
DATA
Y=37.12 x EXP(–TIME/299)
Y=39.9 x EXP(–TIME/285)

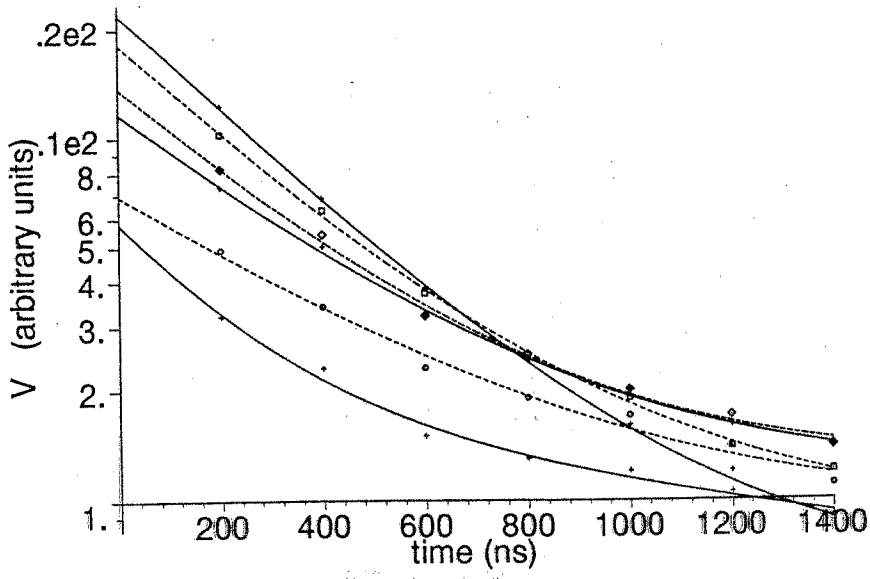



Fig. 9. Decay curves similar to those in figure 7 for a detector irradiated with 1 x $10^{14}$ 55 MeV protons/$cm^2$. The curves are fits of equation (4) to the data points between 200 and 1400 ns, with the curves at the left margin, from highest to lowest, for bias voltages of 45, 30, 20, 15, 10, and 5 V.

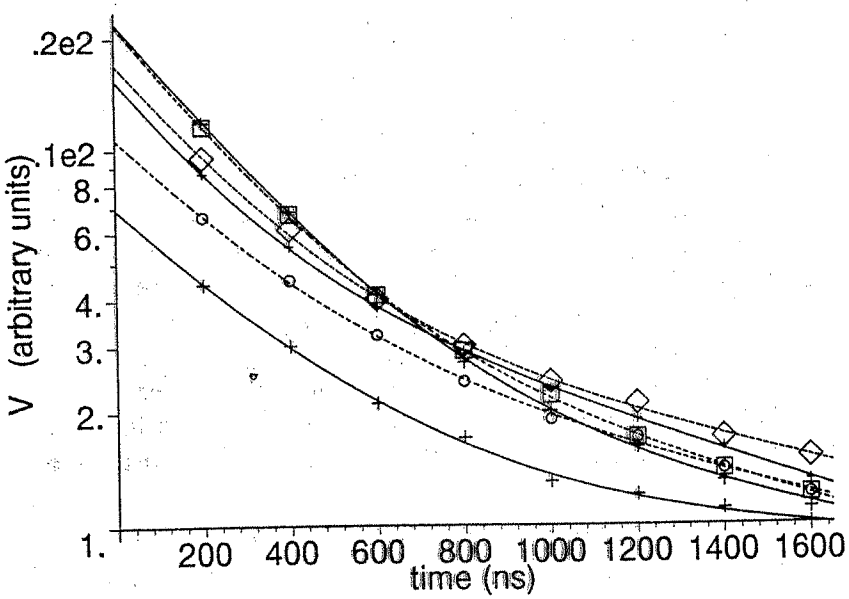



Fig. 10. Decay curves similar to those in figure 7 for a detector irradiated with 2 x $10^{14}$ 55 MeV protons /$cm^2$. The curves are fits of equation (4) to the data points between 200 and 1600 ns, with the curves at the left margin, from highest to lowest, for bias voltages of 60, 40, 20, 15, 10, and 5 V.

Figures 9 and 10 show similar sets of signal decay curves for detectors irradiated with 1 and 2 x $10^{14}$, 55 MeV protons per $cm^2$. In contrast with the curves for unirradiated detectors, there is now a high tail at longer times, easily visible after the initial exponential decrease. This tail may be due to the release of charge from traps produced by the irradiation. If we assume a single dominant trapping time constant, $\tau$, and define

$q_e$ = the charge on the electrode

$q_{e0}$ = the initial charge on the electrode (from the rapidly collected, untrapped charge)

$q_{t0}$ = the initial trapped charge in the cell around the electrode

V = the voltage on the probe

$V_0$ = the initial voltage on the probe (from $q_{e0}/C$, since at t=0, the charge $q_{t0}$ is all trapped)

$V_{\tau 0}$ = the voltage the electrode and probe would have if a charge $q_{t0}$ were deposited on them

R = the resistance of the probe

C = the capacitance of the electrode and probe

then,

$$\frac{dq_e}{dt} = -I_{to-probe} + I_{from-traps} = -\frac{V}{R} - \frac{d}{dt}(q_{\tau 0} e^{-\frac{t}{\tau}}) = -\frac{q_e}{RC} + \frac{q_{\tau 0}}{\tau} e^{-\frac{t}{\tau}} \qquad (3)$$

If we divide each term by C, we have

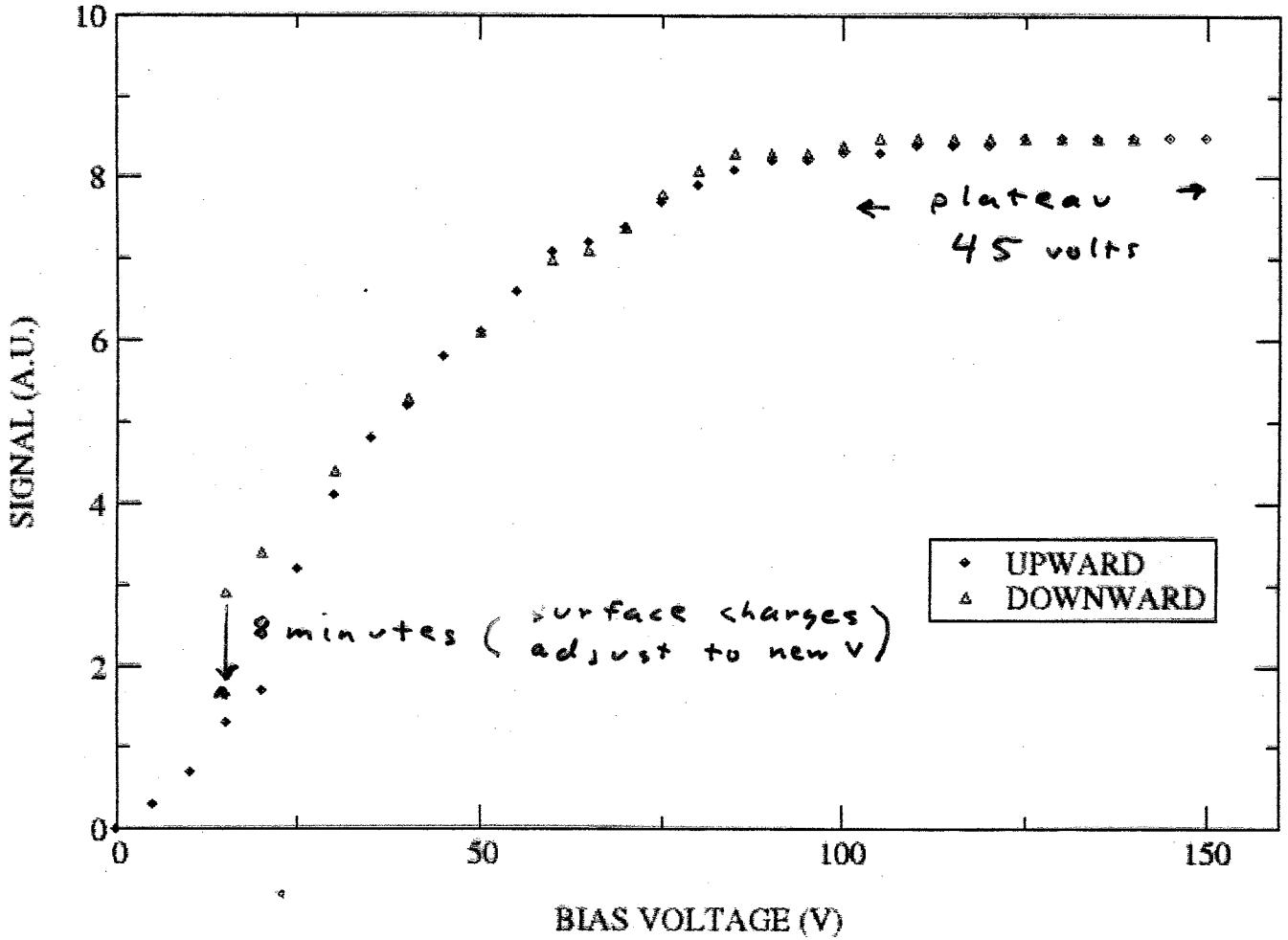
$$\frac{dV}{dt} = -\frac{V}{RC} + \frac{V_{\tau 0}}{\tau} e^{-\frac{t}{\tau}}$$

The solution to this equation is

$$V = [V_0 - V_{\tau 0}(\frac{RC}{\tau - RC})]e^{-\frac{t}{RC}} + V_{\tau 0}(\frac{RC}{\tau - RC})e^{-\frac{t}{\tau}} \qquad (4)$$

# 1E15 55 MeV PROTONS/CM2

## 3D SENSOR, 100 MICRON PITCH, ROOM TEMPERATURE



# Speed -- 3D vs. planar

**1. 3D lateral cell size can be smaller than wafer thickness, so:**

shorter collection distances

**2. in 3D, field lines end on cylinders rather than on circles, so:**

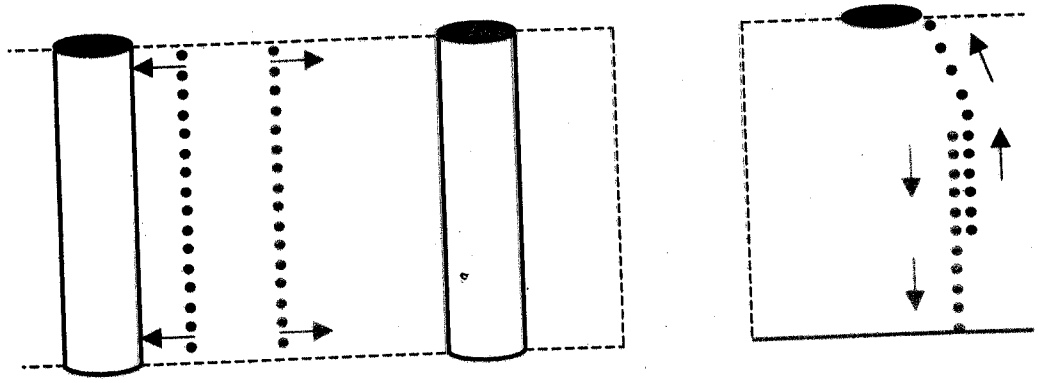
higher average fields for any given maximum field

**(price: larger $C_{electrode}$: we now have 0.2 pF / 121 μm long electrode)**

**3. most of the signal is induced when the charge is close to the electrode, where the electrode solid angle is large, so:**

planar signals are spread out in time as the charge arrives

3D signals are concentrated in time as the track arrives

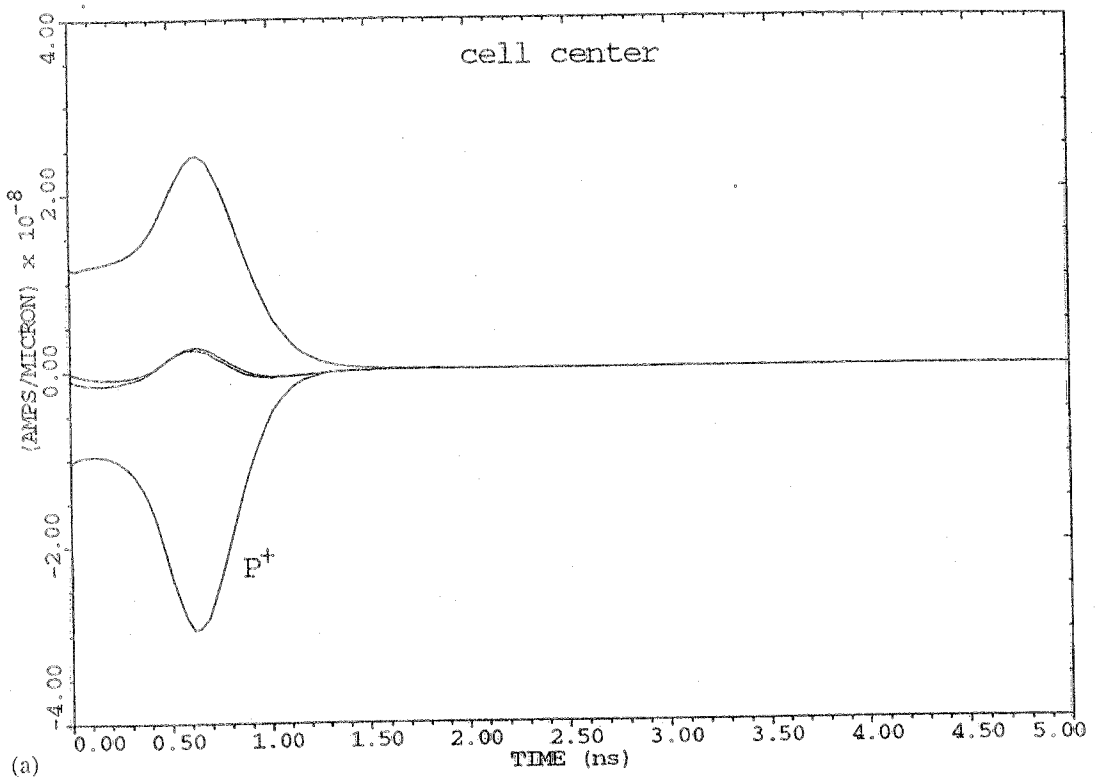


**4. if readout has inputs from both $n^+$ and $p^+$ electrodes,**

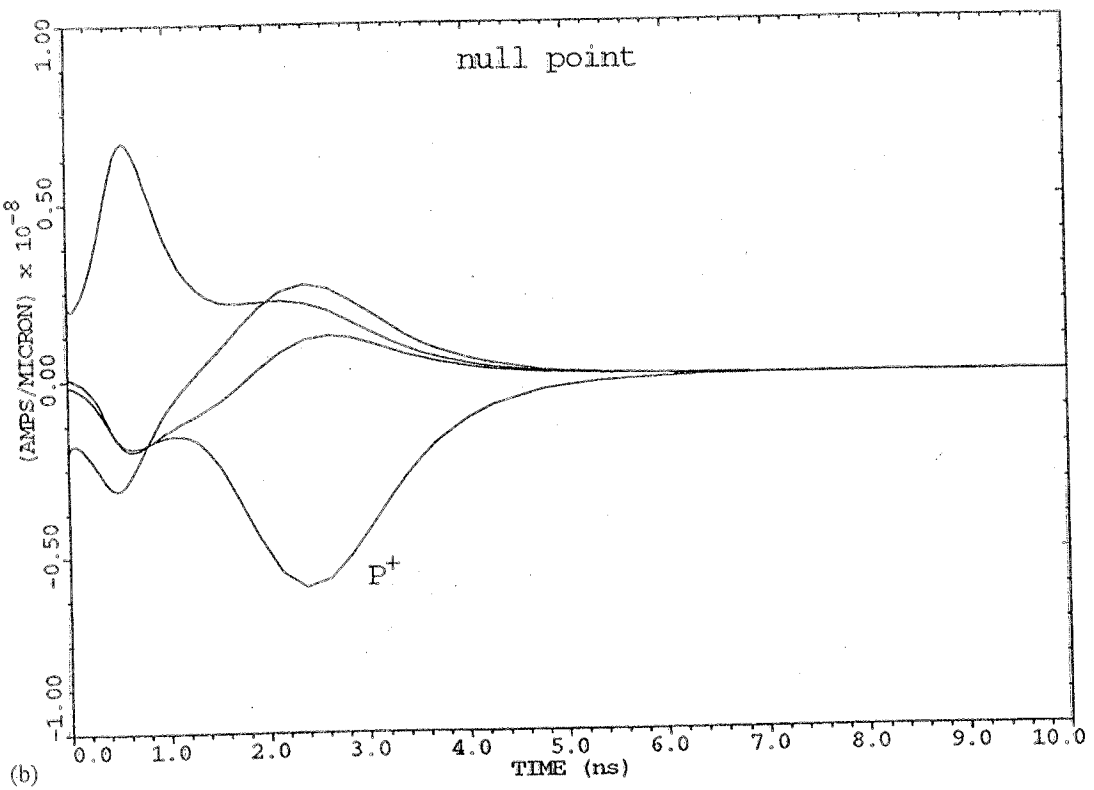
drift time correction can be made

**5. for long, narrow pixels and fast electronics,**

track locations within the pixel can be found




(a)




(b)

Fig. 8. Current pulses on the electrodes from a track parallel to the electrodes (a) through the cell center, and (b) through the null point between two $n^+$ electrodes. The fields are those of Fig. 2(c), $10^{12}$/cc, 10 V. Effects of induced pulses from moving charges and diffusion are included, but not Landau fluctuations or Coulomb forces from the other charges along the track.

NUCLEAR
INSTRUMENTS
& METHODS
IN PHYSICS
RESEARCH
Section A

# A high-speed low-noise transimpedance amplifier in a 0.25 μm CMOS technology

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**Abstract**

We present the simulated and measured performance of a transimpedance amplifier designed in a quarter micron CMOS process. Containing only NMOS and PMOS devices, this amplifier can be integrated in any submicron CMOS process. The main feature of this design is that a transistor in the feedback path substitutes the transresistance. The circuit has been optimized for reading signals coming from silicon strip detectors with few pF input capacitance. For an input charge of 4 fC, an input capacitance of 4 pF and a transresistance of 135 kΩ, we have measured an output pulse fall time of 3 ns and an Equivalent Noise Charge (ENC) of around 350 electrons rms. In view of a utilization of the chip at cryogenic temperatures, measurements at 130 K have also been carried out, showing an overall improvement in the performance of the chip. Fall times down to 1.5 ns have been measured. An integrated circuit containing 32 channels has been designed and wire-bonded to a silicon strip detector and successfully used for the construction of a high-intensity proton beam hodoscope for the NA60 experiment. The chip has been laid out using special techniques to improve its radiation tolerance, and it has been irradiated up to 10 Mrd ($SiO_2$) without showing any degradation in the performance. 

*Keywords:* Deep submicron; CMOS; Transimpedance amplifier; Radiation tolerance; Low temperature CMOS

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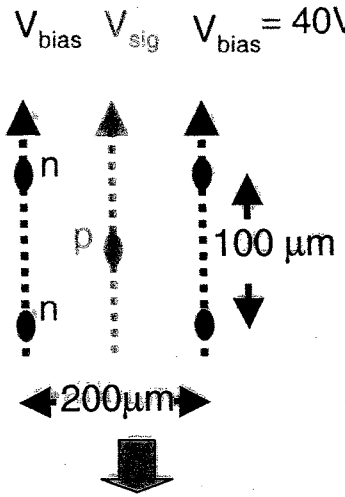
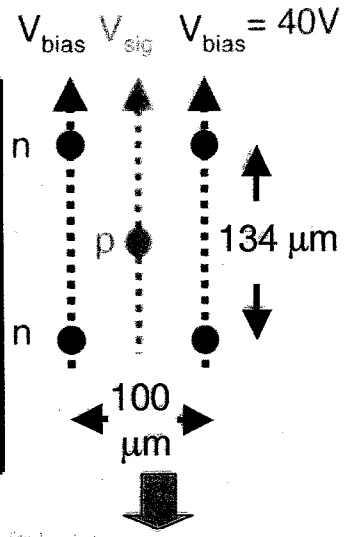
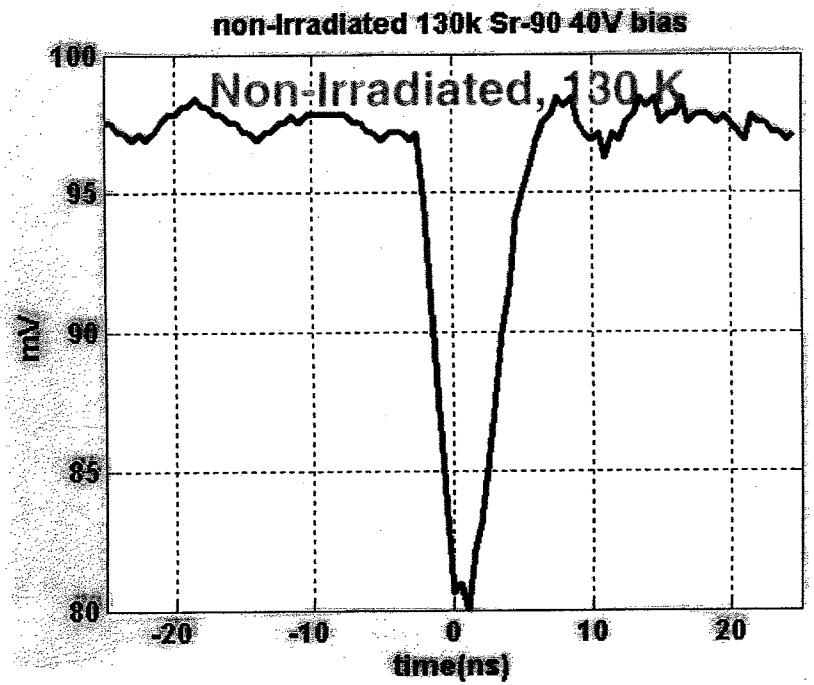
# 3D SENSORS' SPEED

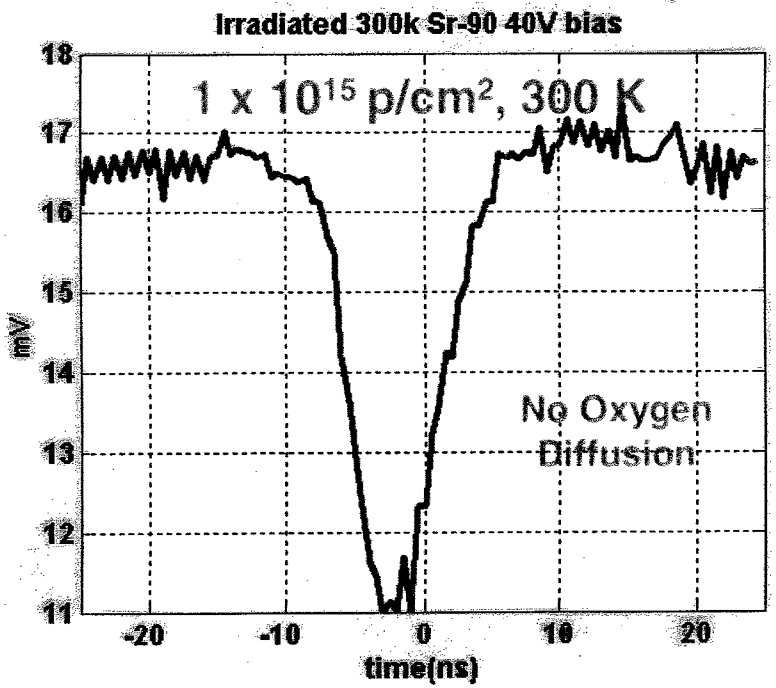
**Thickness=120μm**




| Cell Width | Rise time | T | Fluence |
|---|---|---|---|
| 200 μm | 1.5 ± 0.25ns | 130 K | zero |
| 200 μm | 3.5 ± 0.25ns | 300 K | zero |
| 100 μm | 3.5 ± 0.25ns | 300 K | $10^{15}$p/cm$^2$ |

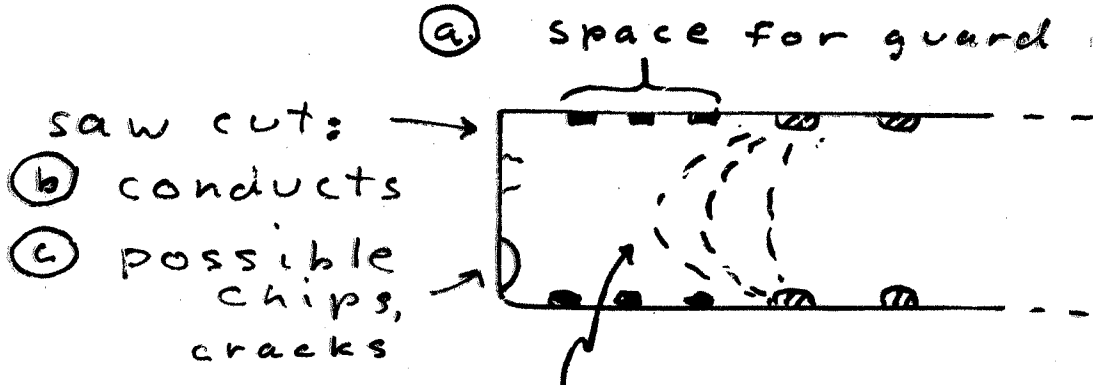


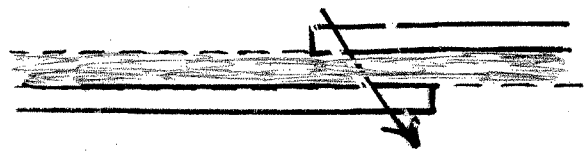



# Active Edges

① planar technology:




ⓔ support thickness + angled tracks may require still more overlap

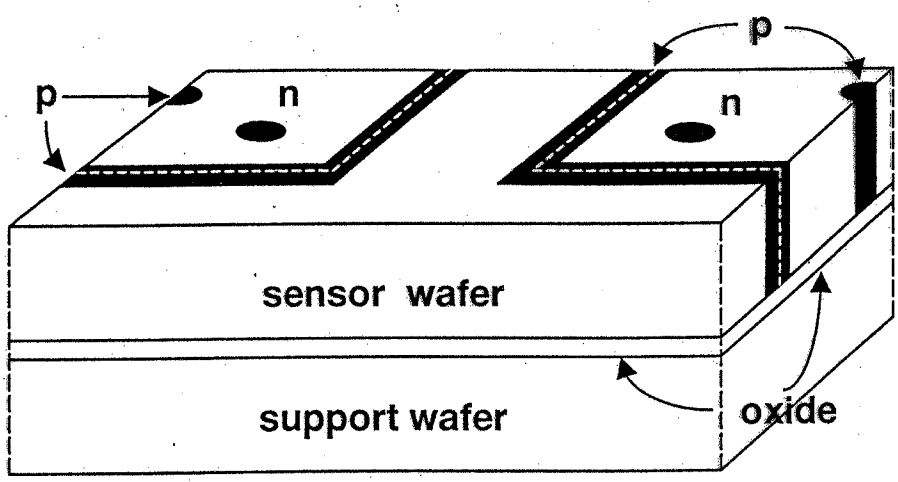


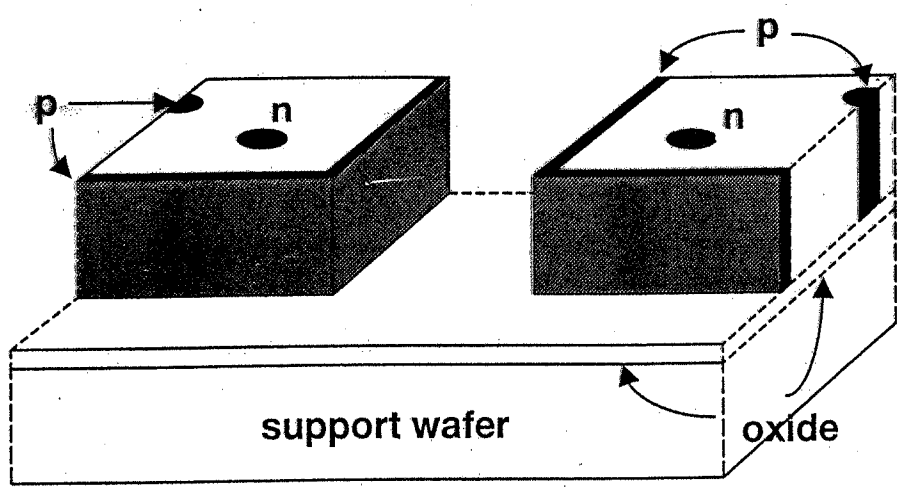
② pianar +

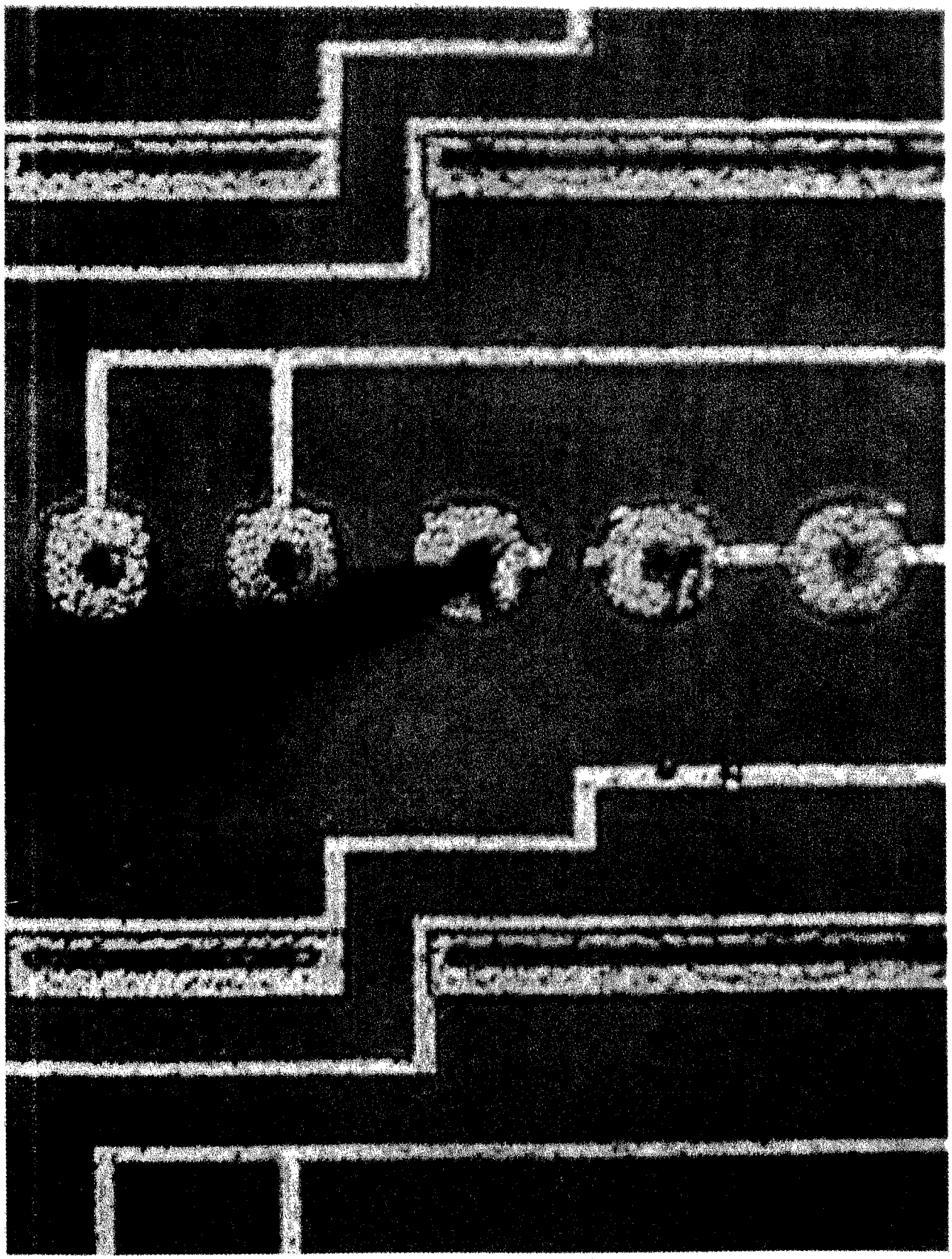
ⓐ mount wafer on support
ⓑ etch edges (no chips)
ⓒ deposit oxide ($SiH_4 + O_2$) (LTO)

③ 3D (no bulging field lines + no chips)

ⓐ mount wafer on support
ⓑ etch edges
ⓒ dope edges to make one electrode

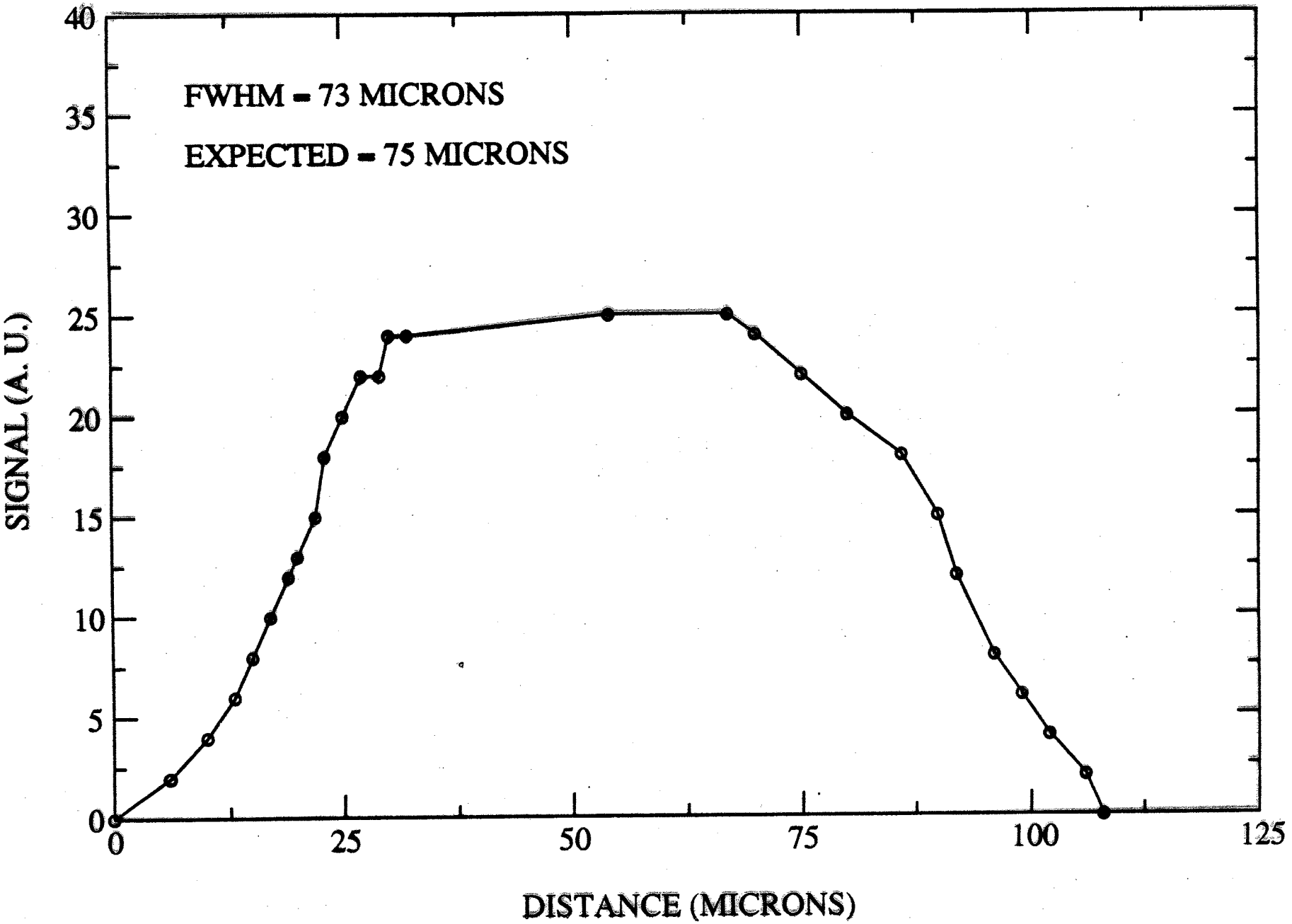

p
p
n
n
sensor wafer
support wafer
oxide


p
p
n
n
support wafer
oxide



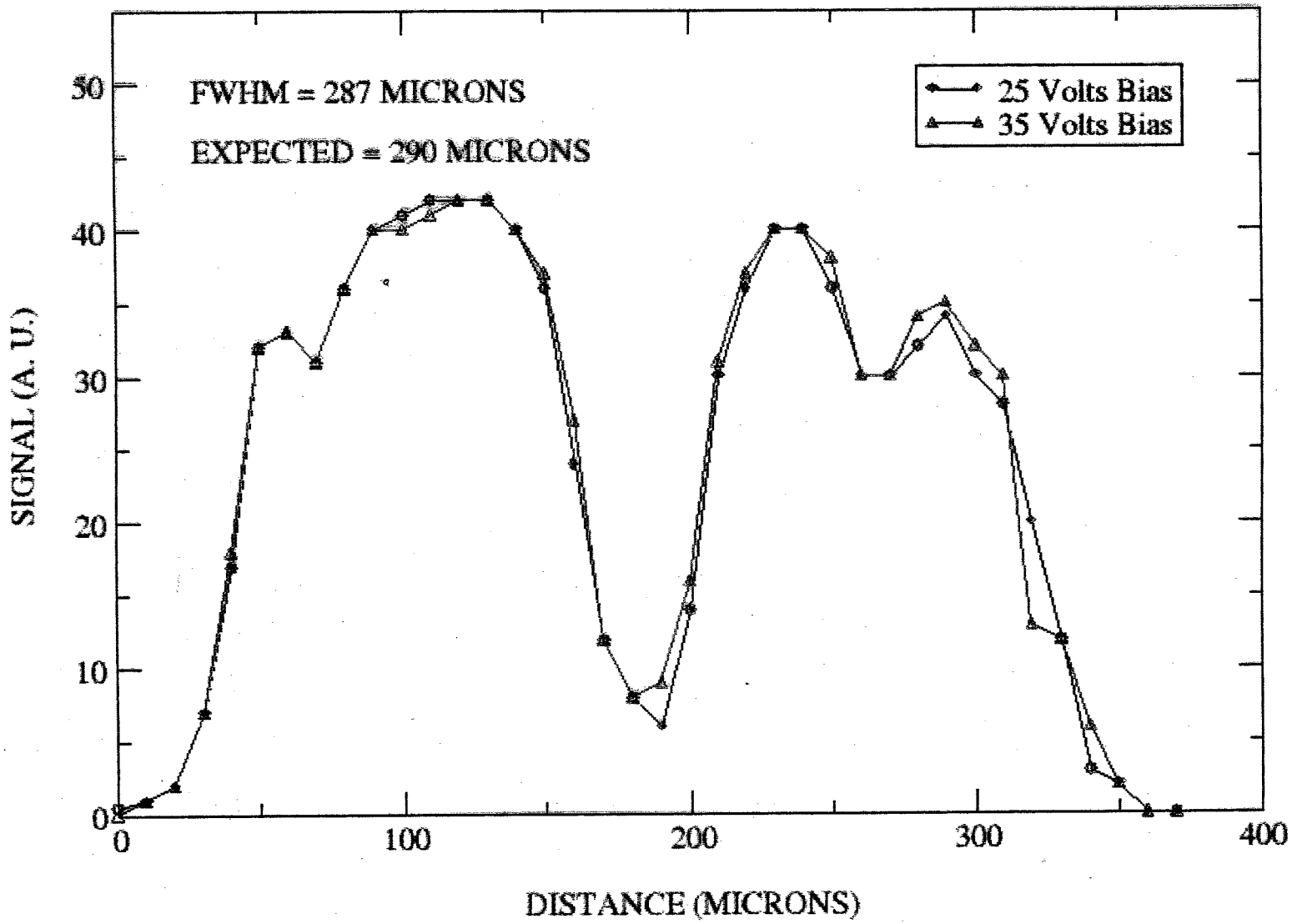
# Y–DIRECTION SCAN

## IR MICRO–BEAM



# X-DIRECTION SCAN

## IR MICRO-BEAM



# CONCLUSIONS

1. THE FIRST 3D DETECTORS HAVE BEEN SUCCESSFULLY FABRICATED

2. THEY HAVE REASONABLE LEAKAGE CURRENTS: ¼ - 1 nA PER $MM^3$ AT ROOM TEMPERATURE

3. THEY DEPLETE AT LOW VOLTAGES AS EXPECTED (TYPICALLY 5 – 10 V)

4. THEY HAVE WIDE PLATEAUS FOR INFRARED MICROBEAM SIGNALS

5. BETA, X-RAY, AND GAMMA SIGNALS HAVE BEEN SEEN

6. A 14 KEV X-RAY LINE FROM A $^{241}Am$ SOURCE FITS A SYMMETRIC GAUSSIAN WITH A SIGMA OF 282 eV

7. A SENSOR WITH 100-MICRON CELL SIZE HAD ITS DEPLETION VOLTAGE INCREASE FROM 5 V TO 105V (WITH A 45 V WIDE PLATEAU) AFTER IRRADIATIION WITH $10^{15}$ – 55 MEV PROTONS / $CM^2$ (PRIOR TO BENEFICIAL ANNEALING)

8. ACTIVE EDGE PREVIEW: AN INFRARED MICROBEAM SCAN SHOWS A SENSOR WITH SETS OF NORMAL 3D CYLINDRICAL ELECTRODES BETWEEN TWO WALL ELECTRODES IS SENSITIVE TO WITHIN SEVERAL MICRONS OF THE WALL ELECTRODE.

9. AMPLIFIER-LIMITED $^{90}Sr$ RISE TIMES OF 3.5 NS AT ROOM TEMP. AFTER $10^{15}$ $P/CM^2$, AND 1.5 NS AT 130° K HAVE BEEN MEASURED

10. THE 2nd FABRICATION RUN HAS STARTED