SCIPP

Silicon Strip Detectors at the SSC, LHC, in Space: Lessons learned…

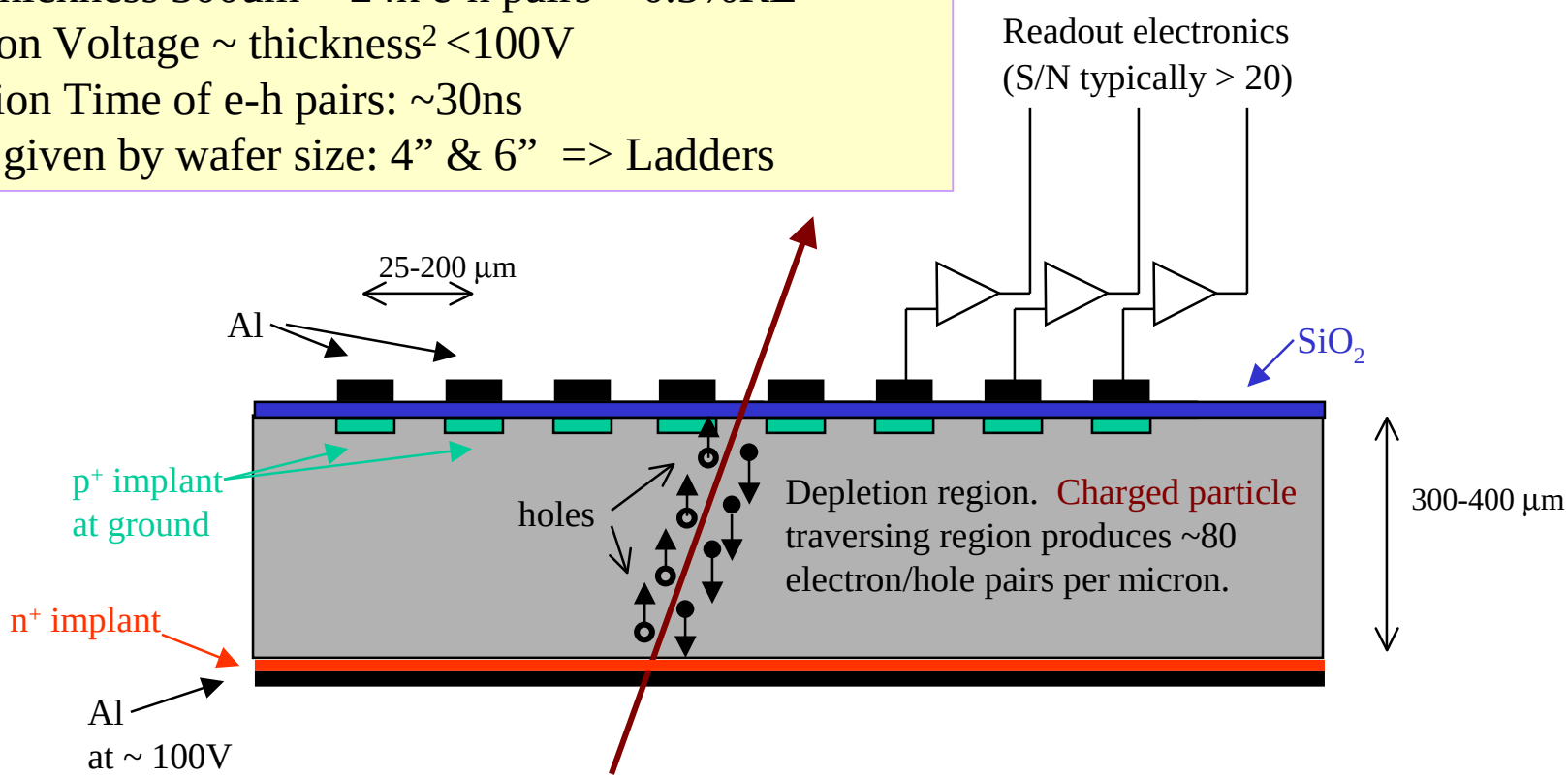
(and right away forgotten)

Hartmut F.-W. Sadrozinski

Santa Cruz Institute for Particle Physics (SCIPP)

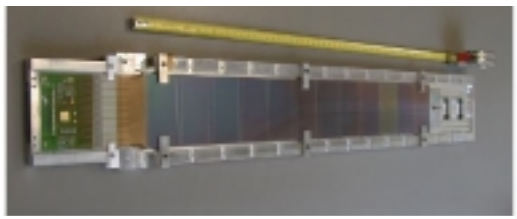
Principle of Silicon Strip Detectors

Reverse Bias of junction: thermal current generation
Scale : Band gap 1.12eV vs. kT = 1/40eV
Cooling needed only in ultra-low noise applications.
Wafer thickness 300um = 24k e-h pairs = 0.3%RL
Depletion Voltage ~ thickness^2 <100V
Collection Time of e-h pairs: ~30ns
Area is given by wafer size: 4" & 6" => Ladders

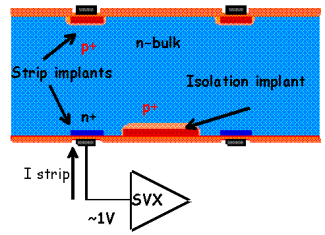


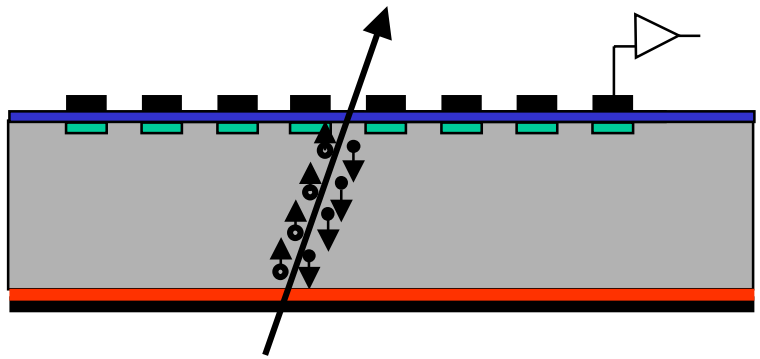
Evolution of Silicon Detectors

Large Area

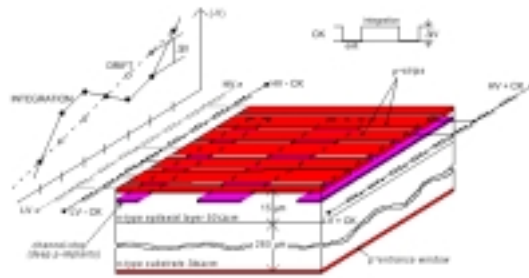


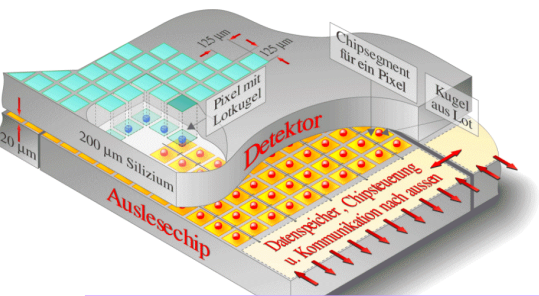
Double-sided



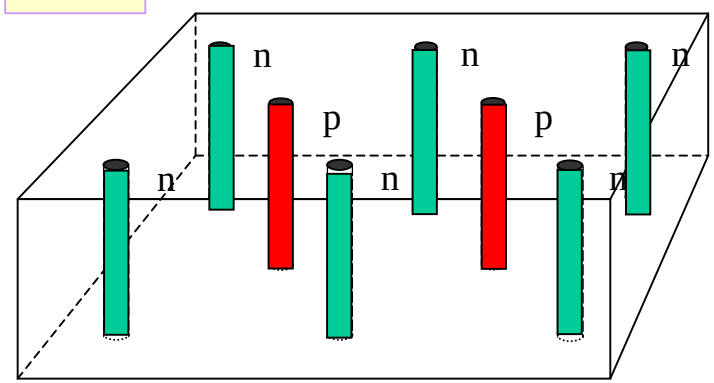


Si Drift

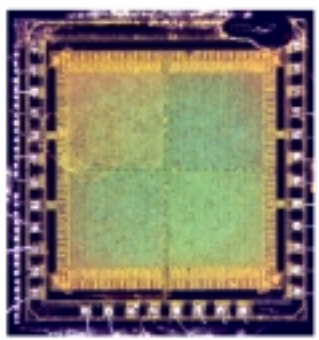




3-D



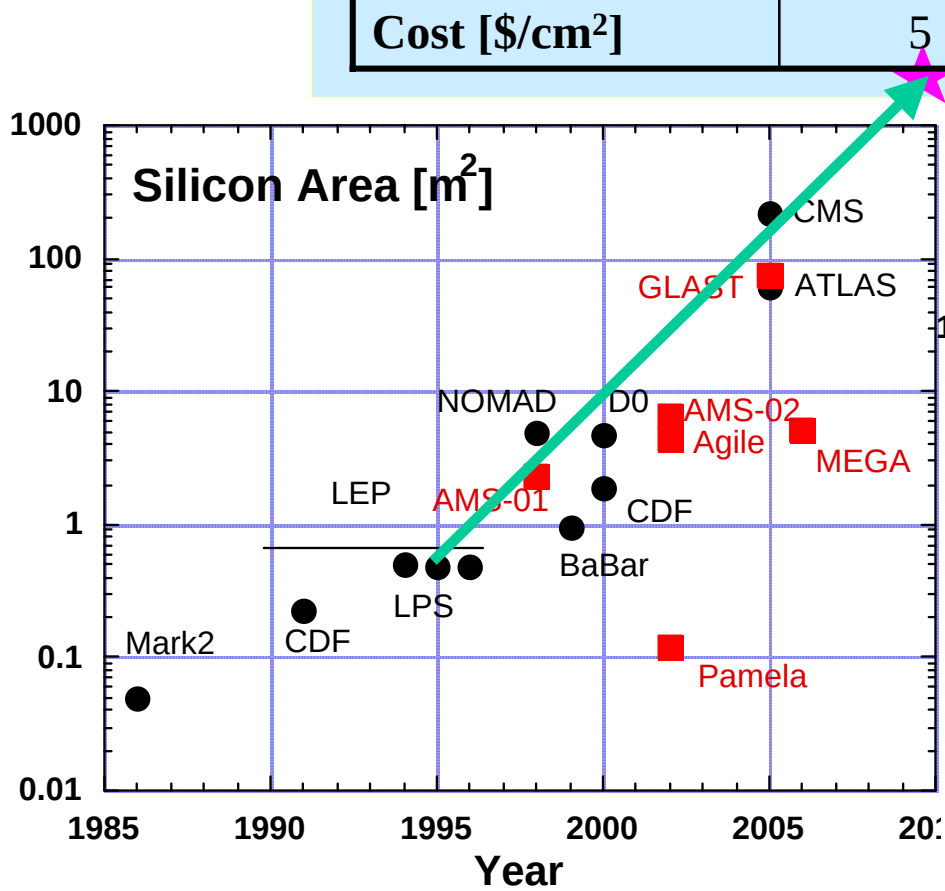
Hybrid Pixels

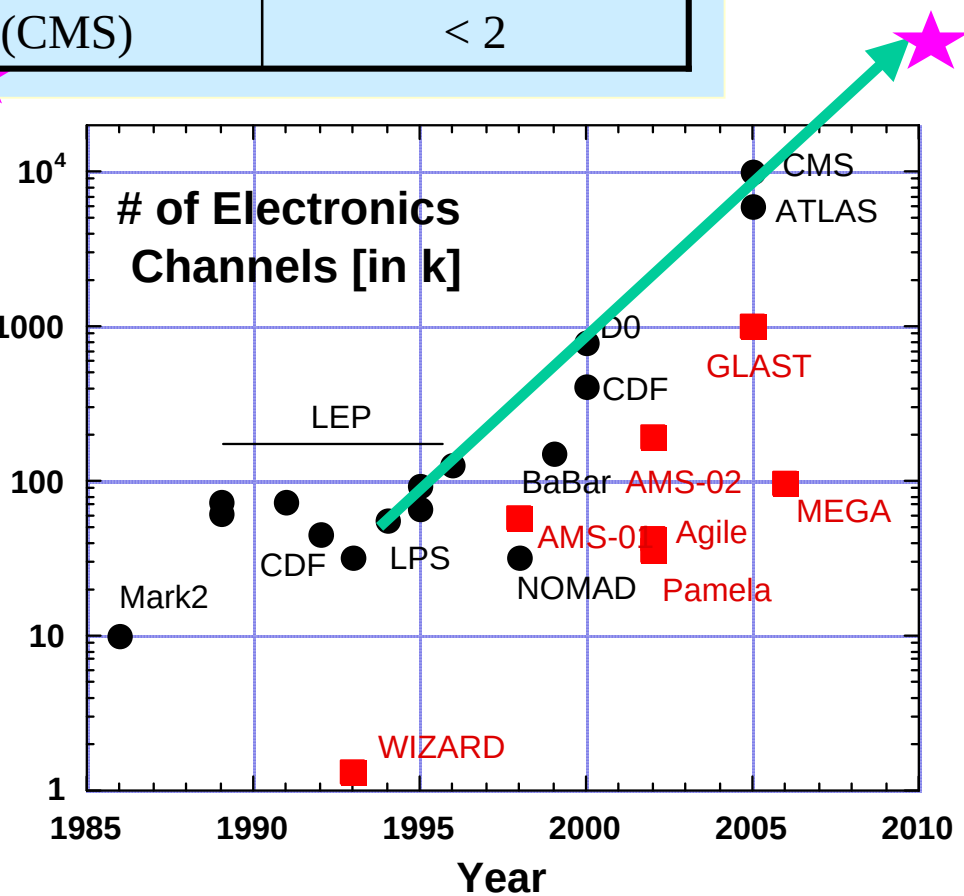


Monolythic:
CCD (SLD), MAP

Moore's Law for Silicon Detectors

Year	2005	2010
Si Area [m^2]	230 (CMS)	2,000
# of Channels	10M (CMS)	100M
Cost [$/$cm^2$]	5 (CMS)	< 2





The Cost of SSD: KISS

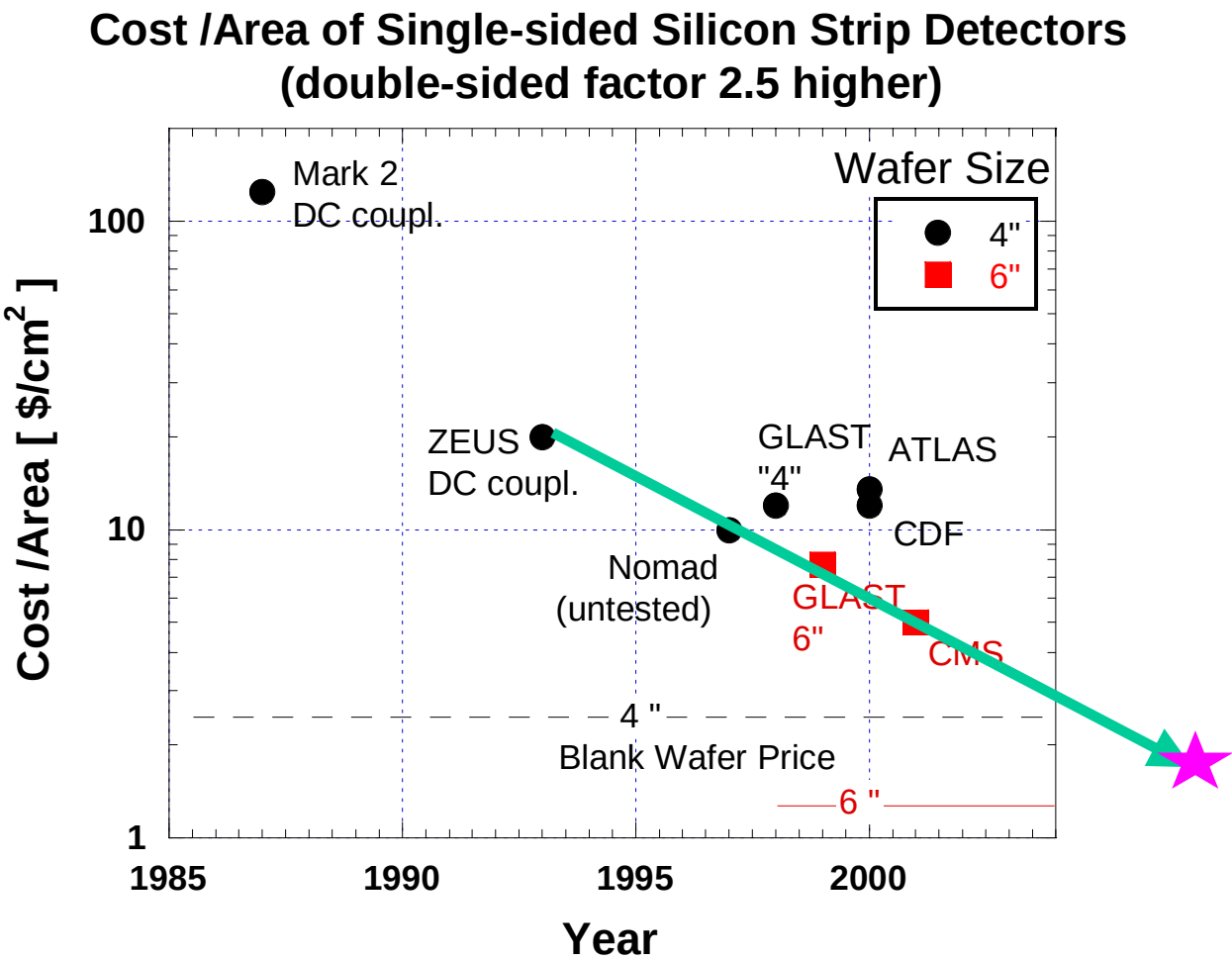
Trends in the Cost of Silicon Detectors

Cost of processing wafers reduced ~ 4x

Increased Area 4" -> 6"
Better utilisation of area
Higher Yield

Improved Quality
e.g. GLAST detectors:
<2nA/ cm^2
<$2*10^{-4}$ bad channels

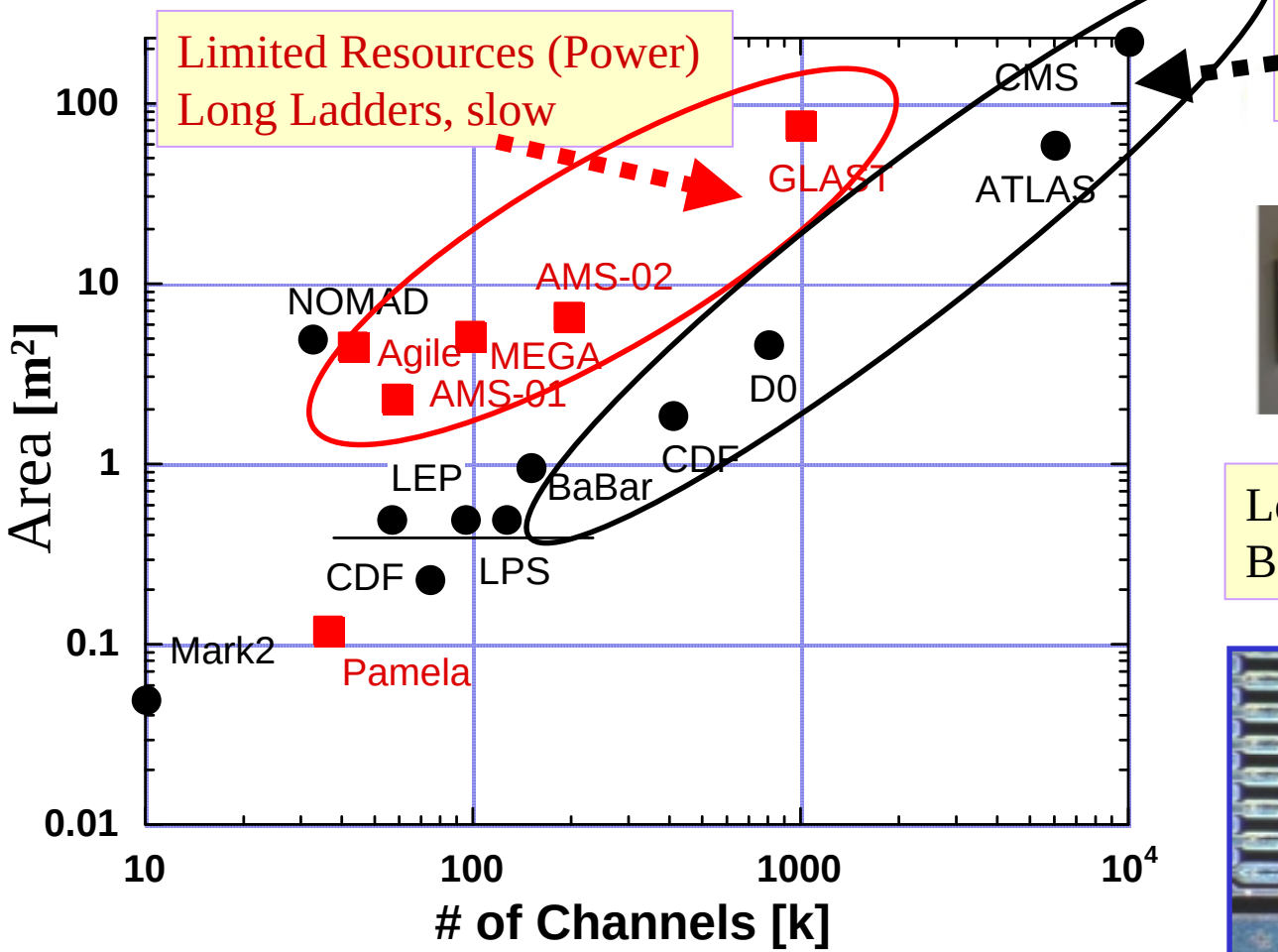
Are Double-sided SSD viable for large system?



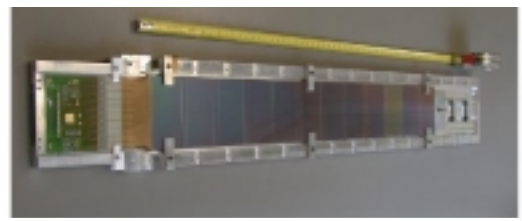
(Guestimates by HFWS)

Design Drivers: Resources and Speed

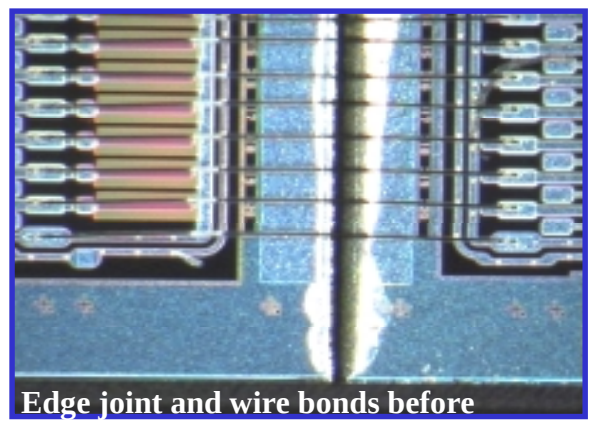
Silicon Area vs. # of Electronics Channels



"Short" strips,
Fast
But power/cooling is not free!



Long Ladders possible with:
Bonding and Encapsulation



SCIPP

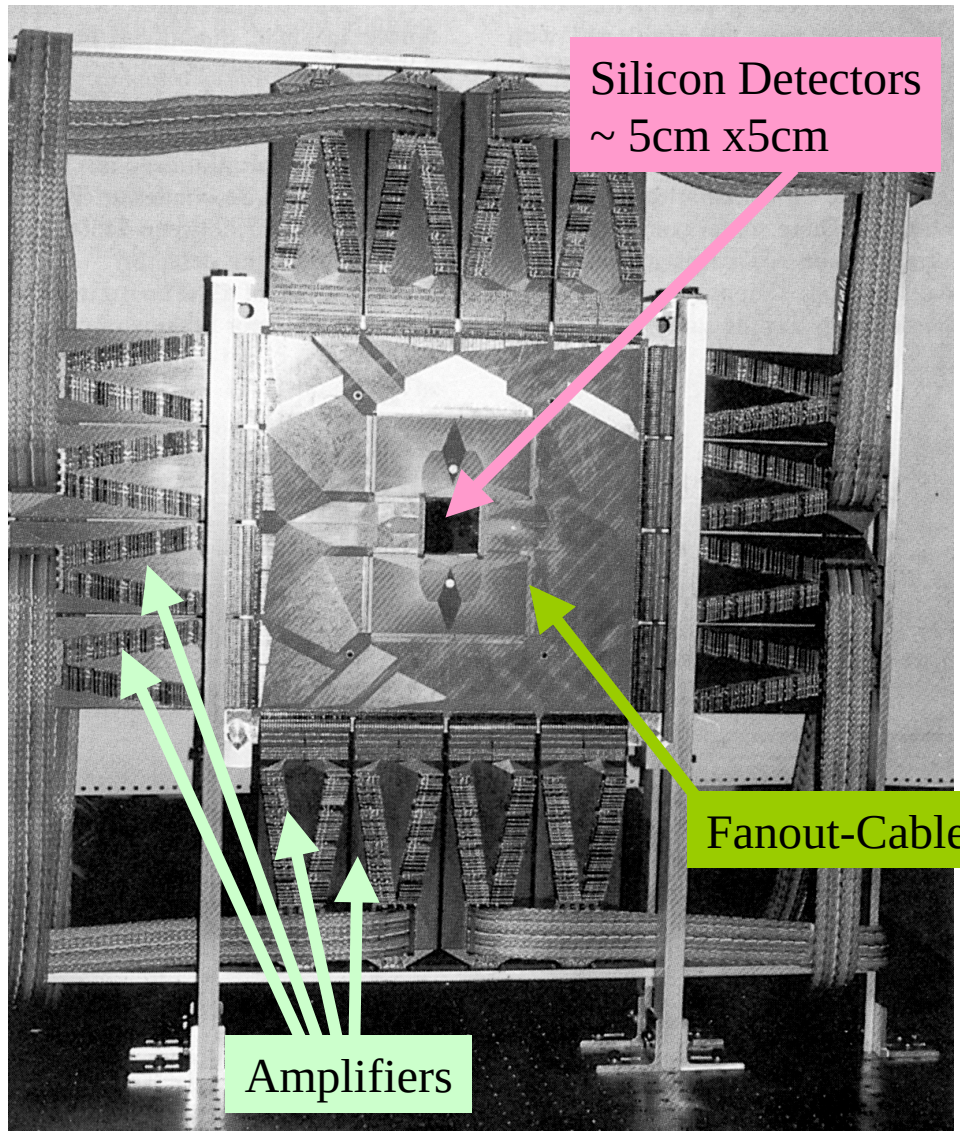
Tracking Milestones: Fixed Target

That's how it all began

Fixed Target experiments with high rates:

Na11 (ACCMOR)
Na14
E706
E691

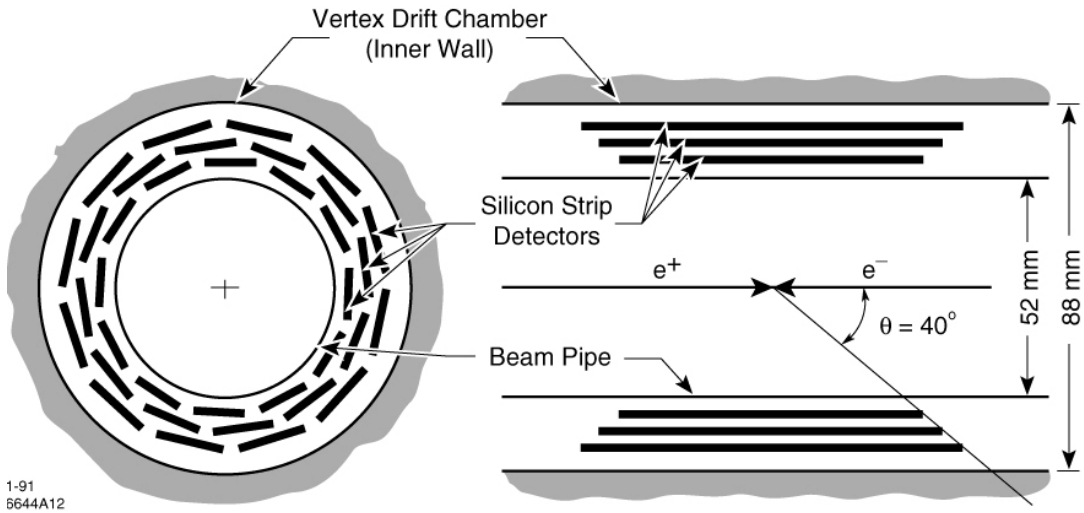
Detect heavy decaying particles through their finite decay distance

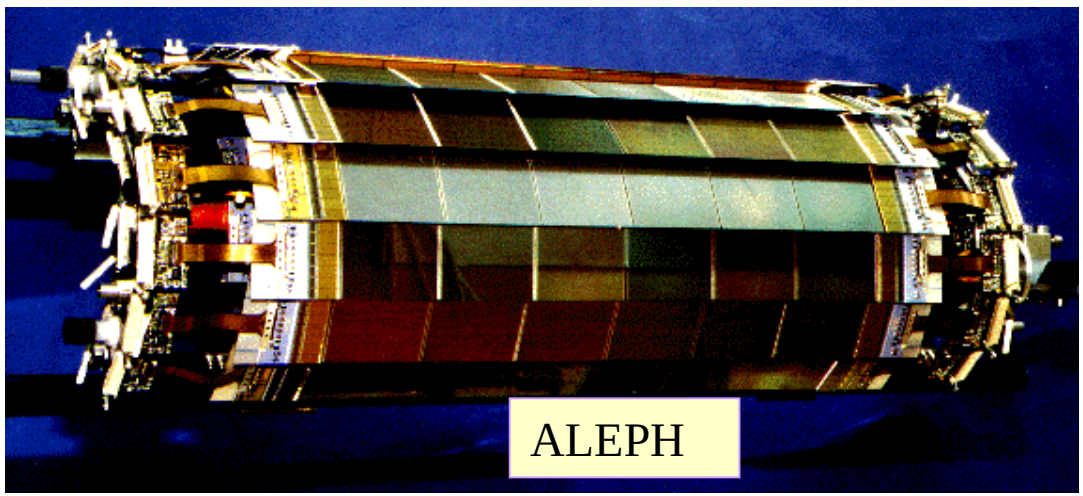


Tracking Milestones: Vertex Detectors

The big step forward in Mark2:
ASIC's (Terry Walker et al)

Vertex Detector Paradigm
ASIC's,
Few thin layers,
Close in.



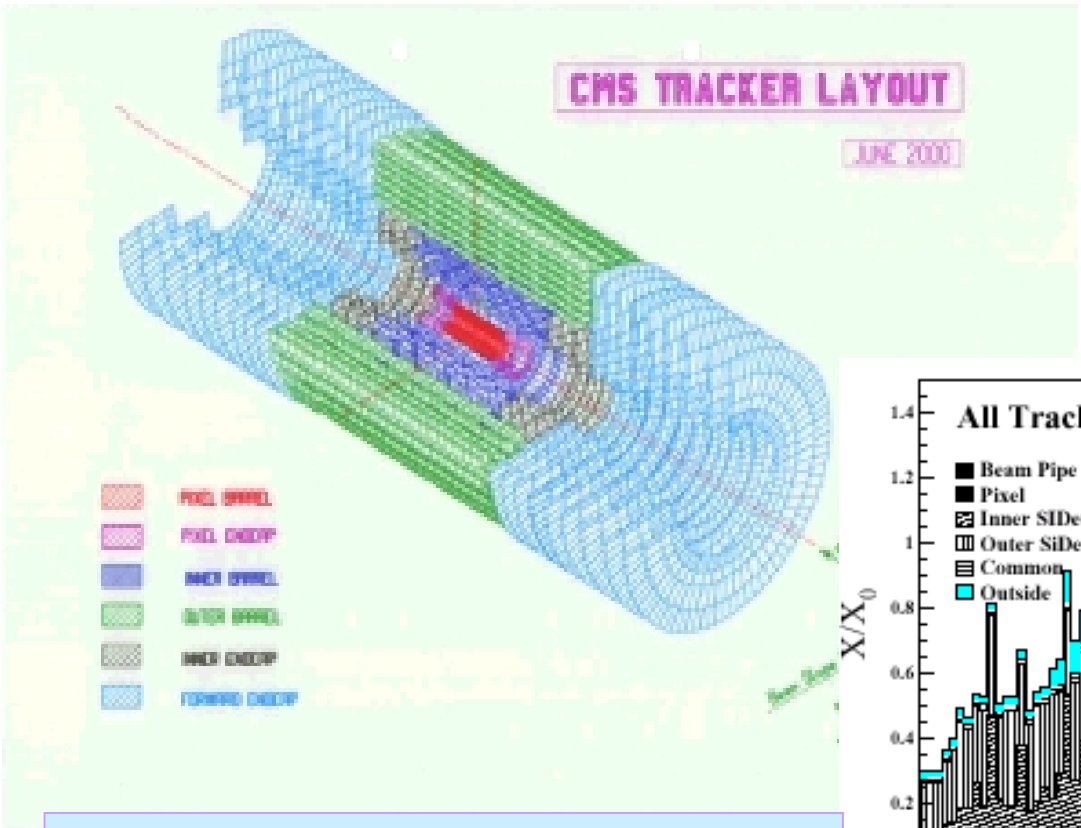


Every LEP Experiment has a Vertex Detectors:

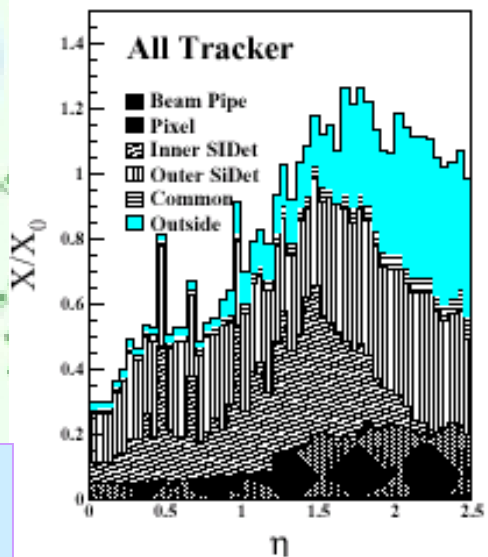
Double-Sided
AC-coupled

SCIPP

Tracking Milestones: Highest Luminosity LHC

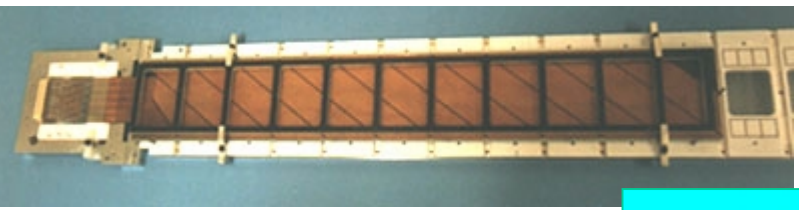


Silicon has arrived:
all Silicon Inner Detector
Si Area 223m^2,
- 6” Wafers -



Continued Paradigm Change:
Outside radius : ~1.1m
~1R.L. in tracking volume

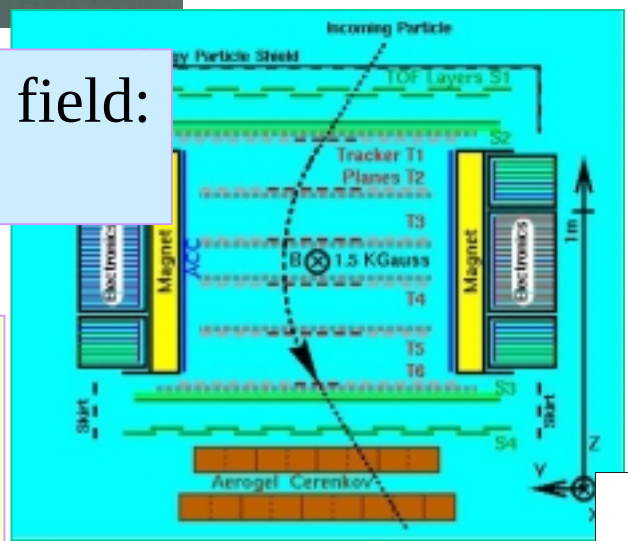
Tracking in Space: AMS

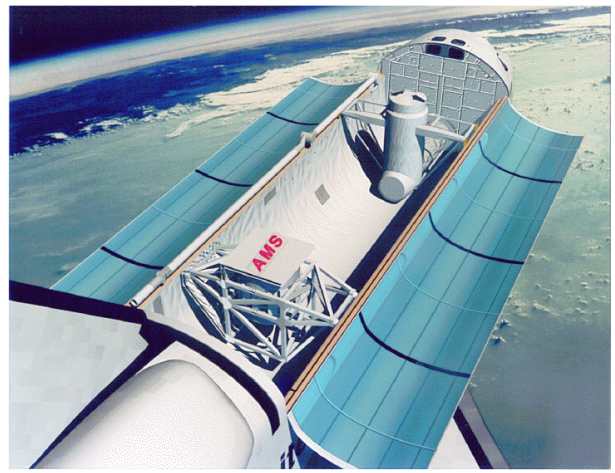


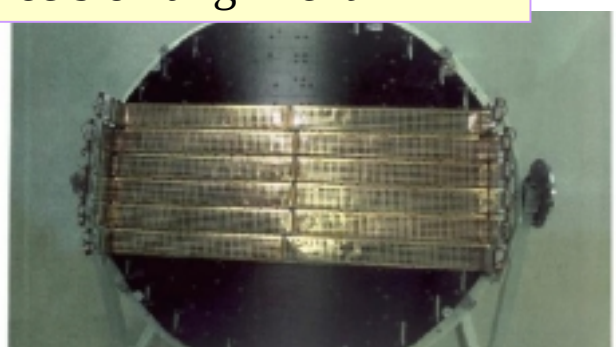
Conservative Adaptation of HEP Technology

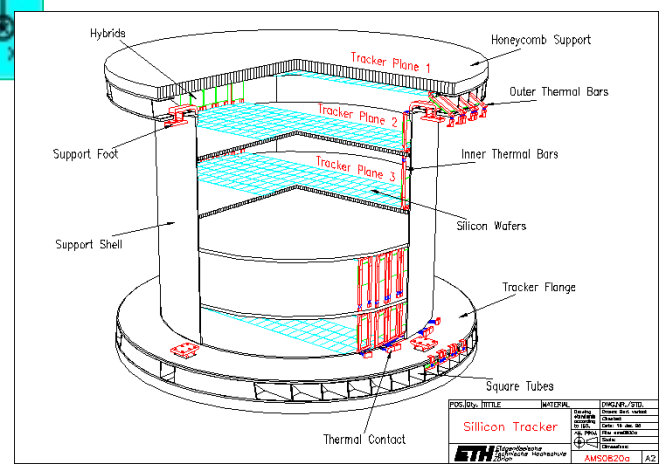
Tracking in Magnetic field: Minimize material

Very long ladders (65cm)
Thin mechanical structures
Electronics outside tracking
Precision alignment









SCIPP

Criteria for large-scale Application:

It's the environment, stupid!

	SSC/LHC	BaBar	GLAST
Time between Collisions [ns]	25 - 40	4	60,000
<ntrack>/Collision	~100	~10^{-5}?	1
Track Rate [kHz]	4,000	0.2?	15
Yearly Dose [Mrad]	1 - hadrons	0.2 - electrons	0.0002 - p
{Radius} [cm]	{30}	{~3}	{n/a}
Cooling	Evaporative	Liquid - FEE	Conductive
Temp [^{o}C]	-17	10	15 - 25
Biggest Headache	Cooling of SSD Radhard ASICs	Low p, Azimuthal Dependence of Radiation	SEE Passive Cooling

SCIPP

Criteria for large-scale Application: KISS

	ATLAS	BaBar	GLAST
Strip Resolution [μm]	25	10	60
Inner/Outer Radius [cm]	30/52 (Pixels 4/14)	3/14	"3cm"
# of Layers	2 x 4 (+- 40mrad) Pixels 3	5 (0, 90°)	2 x 18 (0, 90°)
# of Detectors	SS 16,000 (4")	DS 340	SS 10,000 (6")
# of Modules	4,000	52	300
# of Assembly houses	3+7	~3	1 FEE (Indu.) 2 Trays (Indu.)
Method of Assembly	Optical	Mechanical?	Mechanical
Interfaces: mech Electrical Data	Staves/Cooling Pipe Stave 2 LED / 2 Modules	Cylinders Hybrids G-Link/Module	Tower Trays Tower Cables Tower cables

Tracking Milestones: Highest Luminosity LHC

ATLAS: Silicon Tracker

Simple Detectors, Optimized Electronics

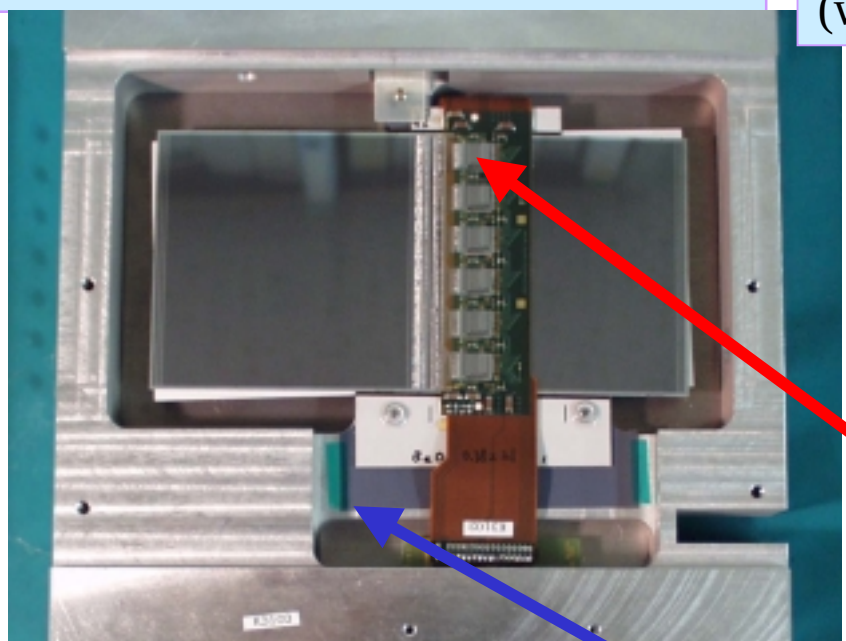
Thermal management

Change in Paradigm:

coverage of large area

electronics inside tracker volume

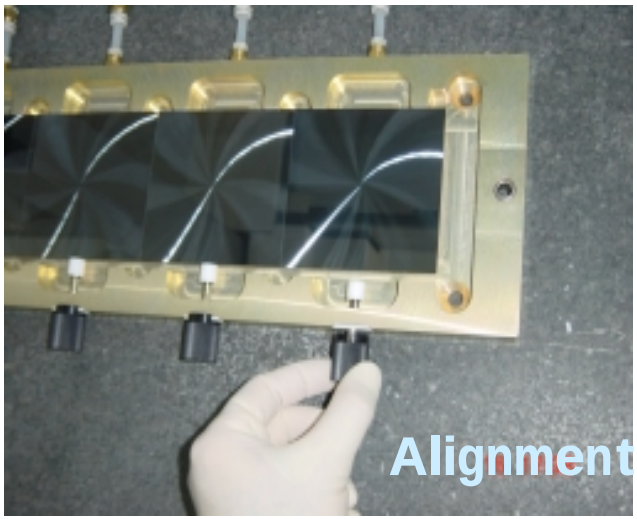
One module 2% R.L., SSD only 0.6%,
(without Services!). ARE THIN SSD VIABLE?

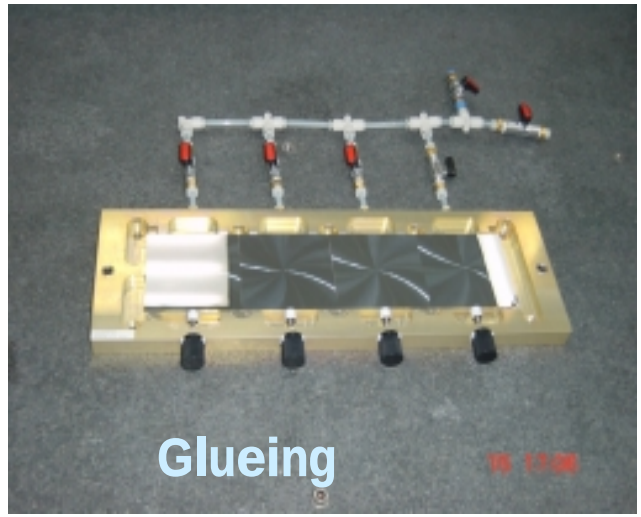


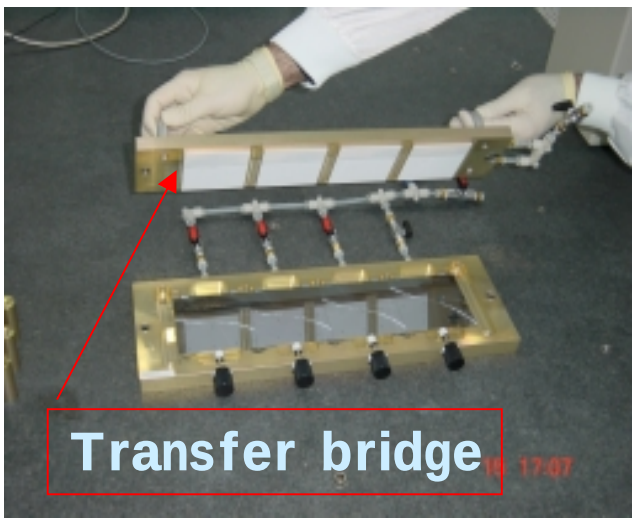
Temperature Range :

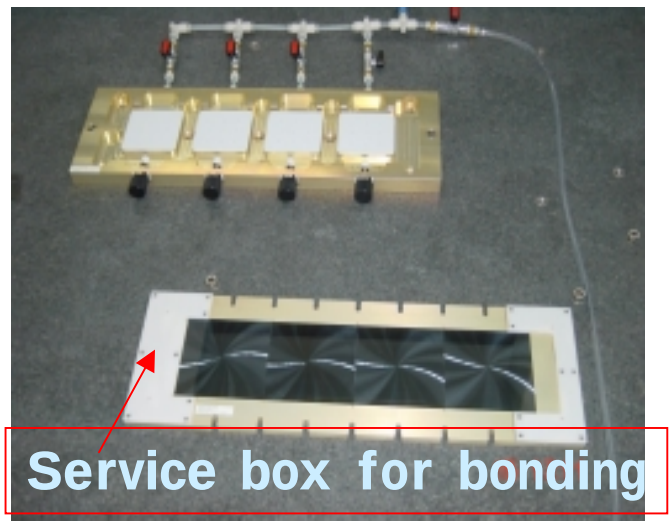
-17°C (cooling pipe) to +16°C (ASICs)

GLAST: Ladder assembly: Mechanical only

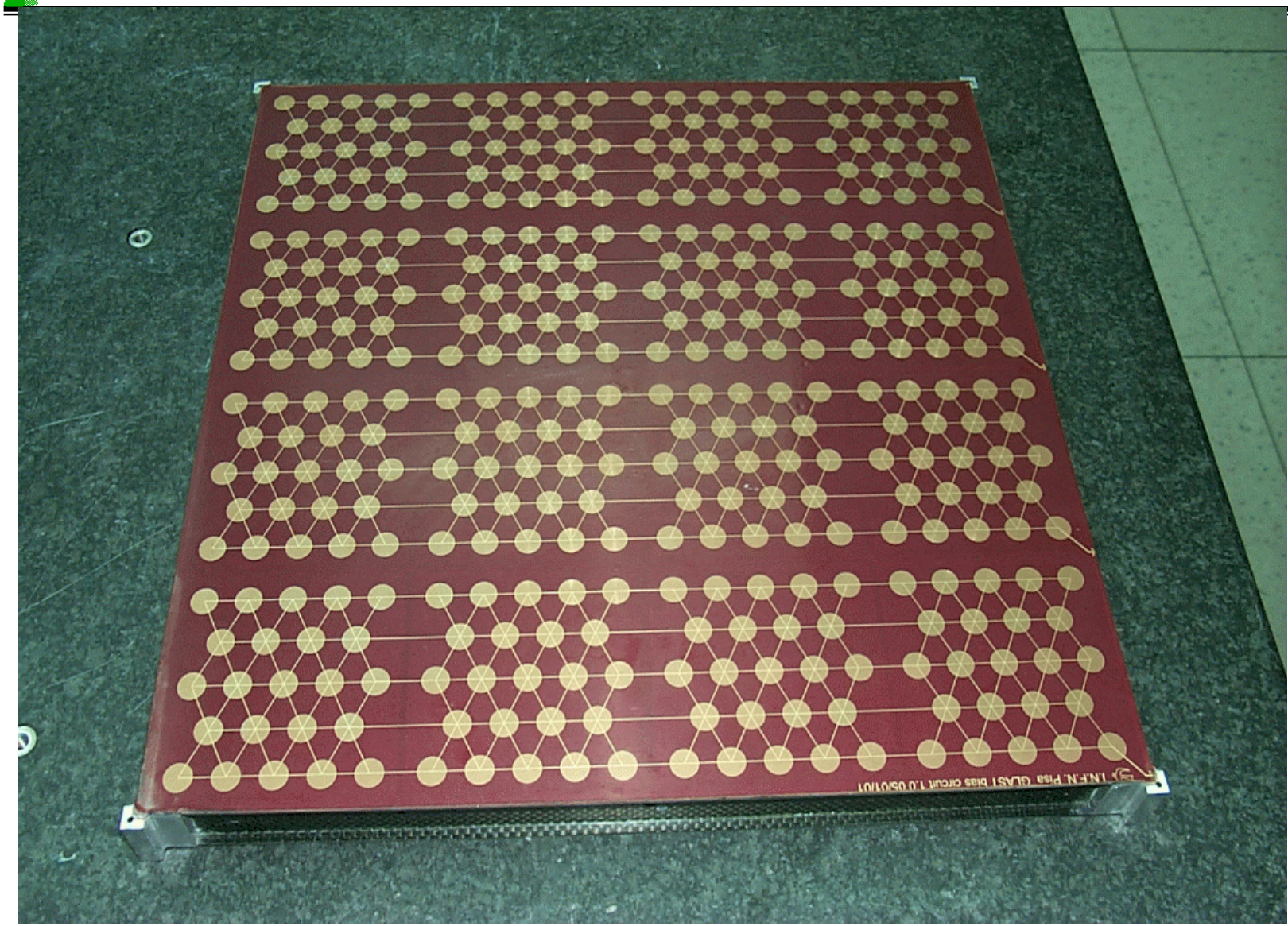




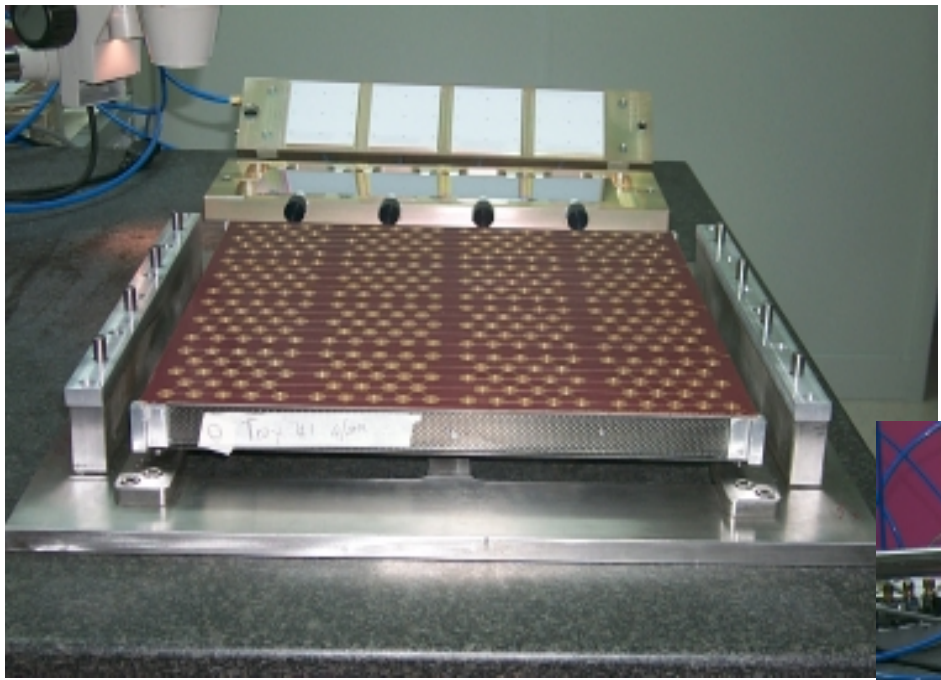


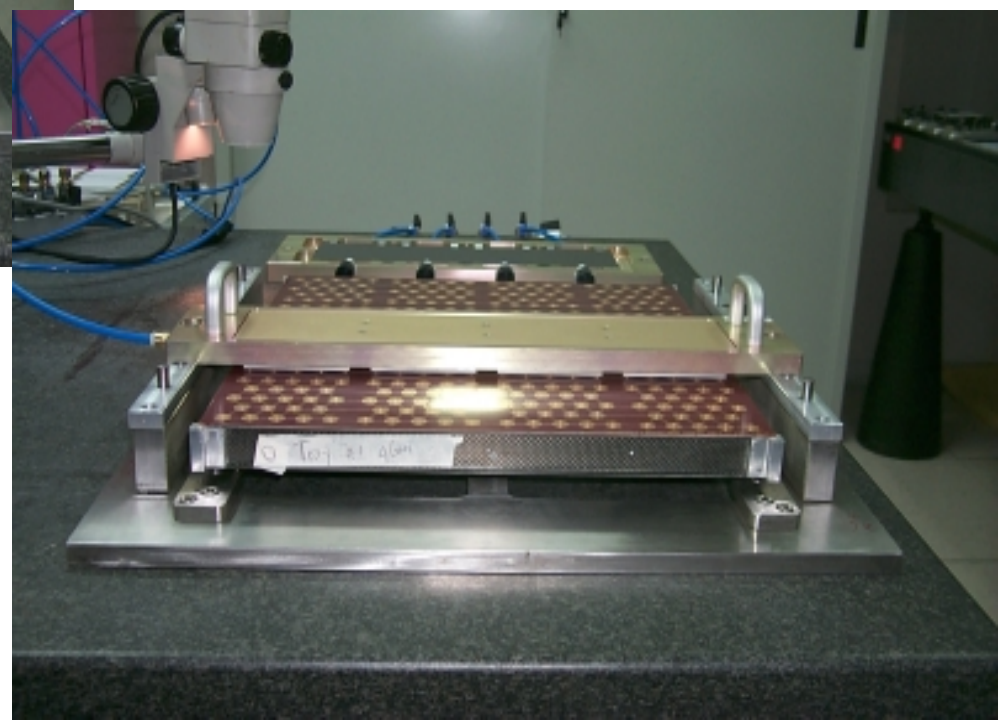


SuperGLAST tray

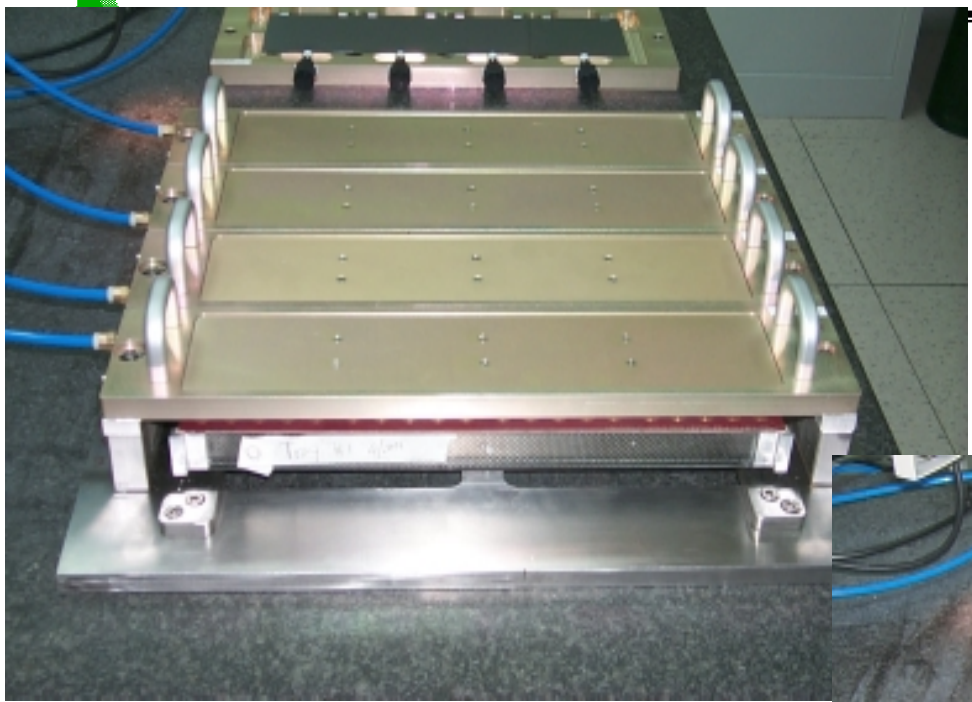


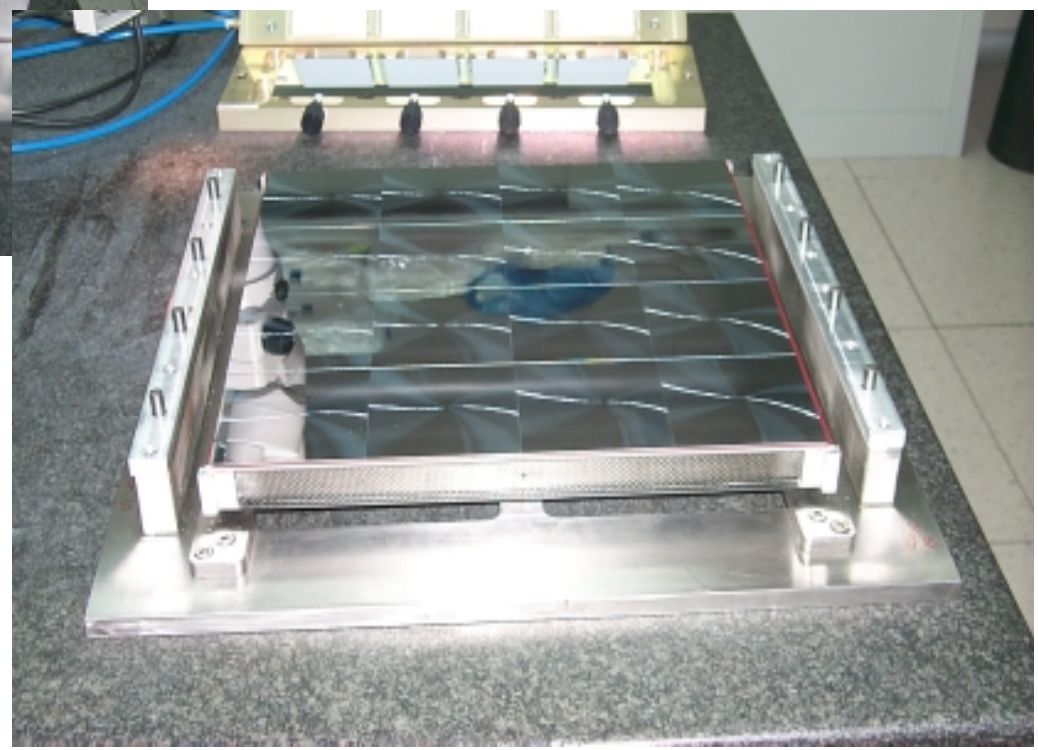
GLAST: Placement of ladders on trays





GLAST: Placement of ladders on trays





SCIPP

SDC/ATLAS Ideas and what happen to them:

	Pro	Con	Accepted/Rejected	
Short Strip SSD L ~ 1 cm	"best noise performance"	Power, Interconnects	R: "long" strips 12cm better	ok
Double-sided SSD	Low mass, space point	Operation, Rad damage	R: Expensive Risky (CDF)	ok
N-side SSD	Mitigates Rad. damage	Cost	R: Expensive, exclusive	bad
Replace Staws by one layer of SSD	Good resolution, No 30% occupancy	No PID	R: No role for straw collaborators	bad
Evaporative Cooling	Self-regulating	open, Isobutane	R: too risky	ok
Binary Ice Cooling	Self-regulating	Ice blockage	R: NO H2O in ATLAS	?
Evaporative Cooling	Self-regulating	Does it work	A: pressure group	?
PG Sandwich Module	Self-heating solved	More mass?	A: safe solution	ok
Kapton Hybrid	Low mass, Industry	Is it stable?	A: only working solution	ok
Binary Readout	Simple, low power	Need more info?	A: lower power, cost (size)	ok
Analog Readout	All info kept, resolution	DAT nightmare	R: more power, cost, DAT	ok
Bipolar ASICs	Elegant, Rad hard	Yield	A: Cost, Rad Hard	?

Cave dinares, cave regentes, cave collaborentes

SCIPP

Good-Bad SDC/ATLAS Ideas

Radiation tolerant detectors:
http://scipp.ucsc.edu/~hartmut/IEEE_97/IEEE_97_HI_LUM.ps

PG Sandwich:
http://scipp.ucsc.edu/~hartmut/spgs_ieee.ps

Short strips
SCIPP SDC Tracker Subsystem Reports
SCIPP 89-39, 90-30, 91-28

Cooling:
SCIPP SDC Tracker Subsystem Reports

Kapton Hybrid straddling the SSD:
Taka Kondo's 2001 IEEE talk

Si Layer at large radius instead of 50 layers of straws
Vancouver SSC Workshop SCIPP 89-50

SCIPP

Criteria for large-scale Application:

Flexibility

- Adapt to Environment, Scale
- Use Conservative Approach
- No New Technologies (LOMTM)

Modularity

- Clean Interfaces
- Low risk in Performance and Schedule
- Pre-test parts, integrate as late as possible

Redundancy

- No single-point failures

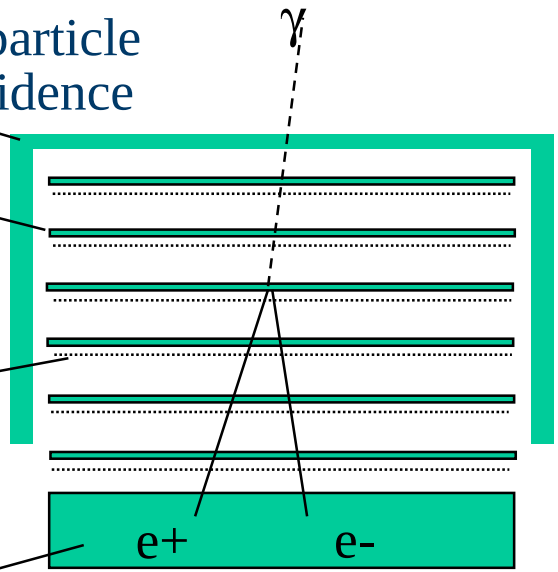
Q/A

- Parts Selection
- Involve Industry
- Procedures
- Early R&D, work with vendors
- Testing

Hartmut F.-W. Sadrozinski , SCIPP, UC Santa Cruz

GLAST Detector Concept: Pair Conversion Telescope

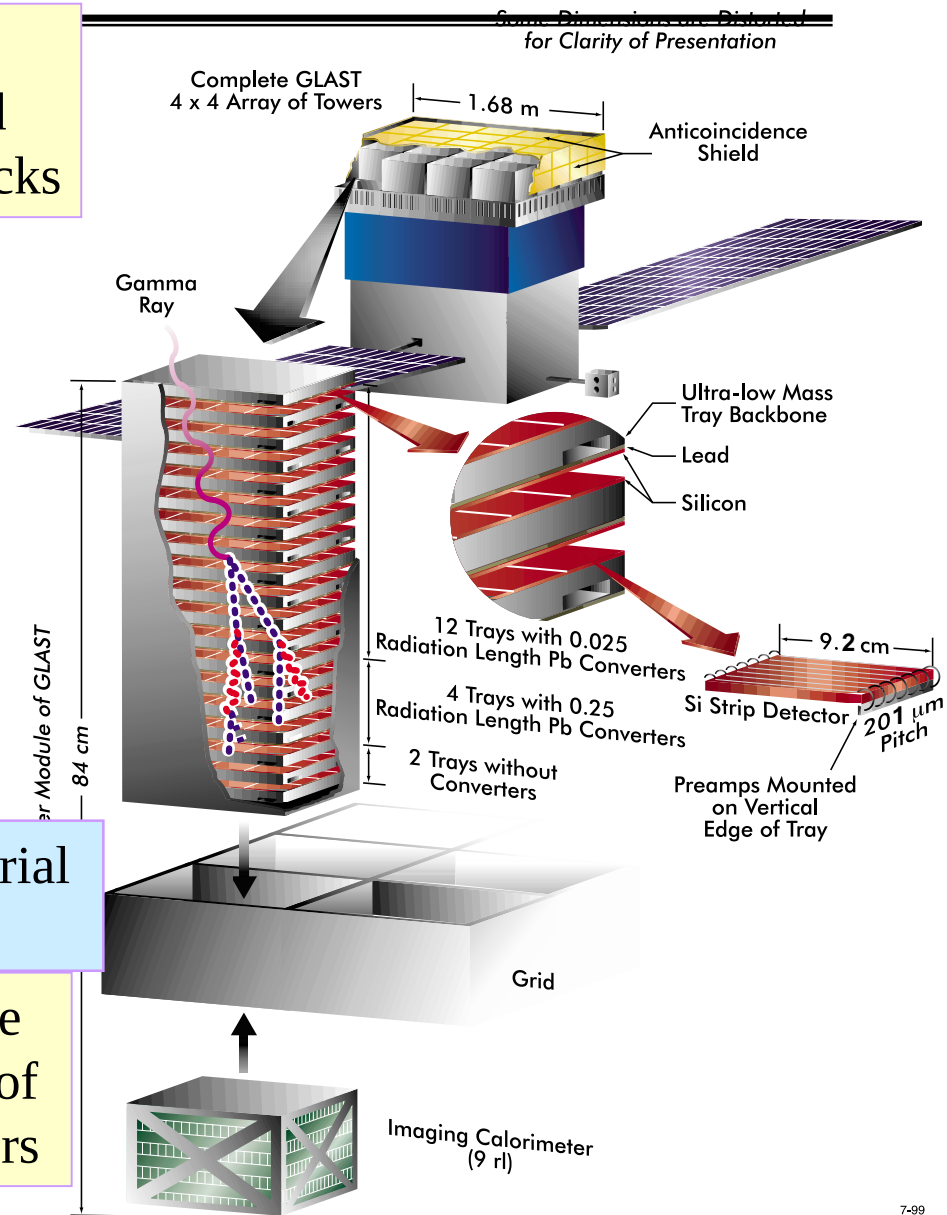
Gamma-rays convert into e^+e^- pairs,
are tracked and their energy measured
Gamma is reconstructed from e^+e^- tracks



New Paradigm:Add material into tracking volume:

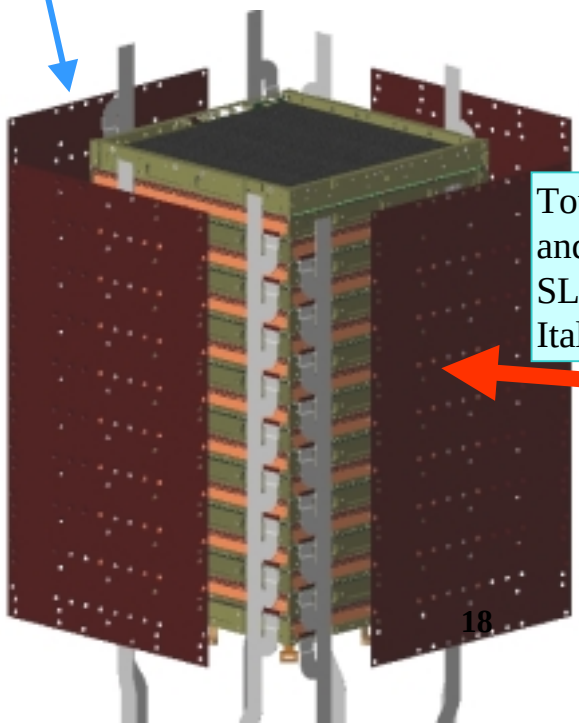
Converter Thickness t
Conversion Probability ~ t
Pointing RMS ~ √t

Maximize Number of Converters



GLAST TKR Flight-Tower Design & Assembly

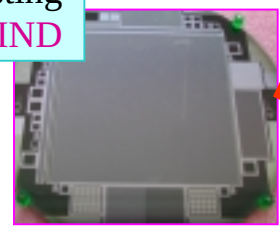
Tower Structure (walls, fasteners)
Engineering: SLAC, Hytec
Procurement: SLAC IND



18

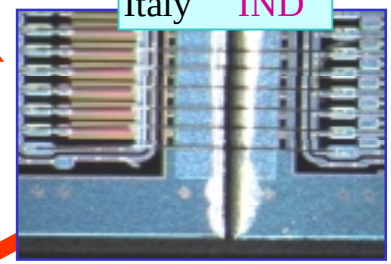
Tower Assembly and Test
SLAC (2)
Italy (16)

SSD Procurement, Testing
Japan, Italy, SLAC IND

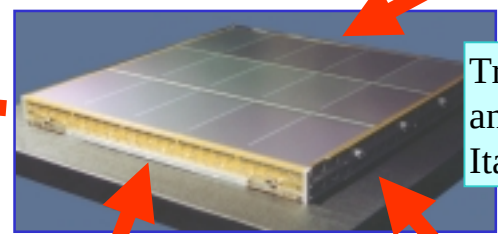


10,368

SSD Ladder Assembly
Italy IND

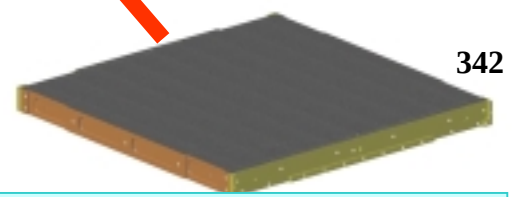


2592



342

Tray Assembly and Test
Italy IND



342

Composite Panel & Converters
Engineering: SLAC, Hytec, and Italy
Procurement: Italy IND

Cable Plant
UCSC IND

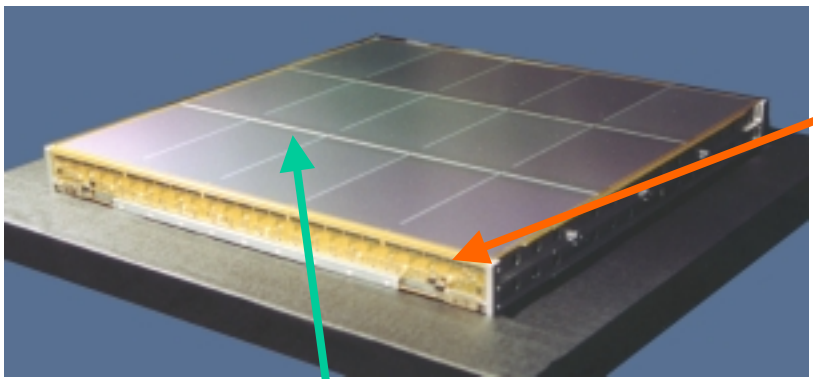
Electronics Design, Fabrication & Test
UCSC, SLAC IND

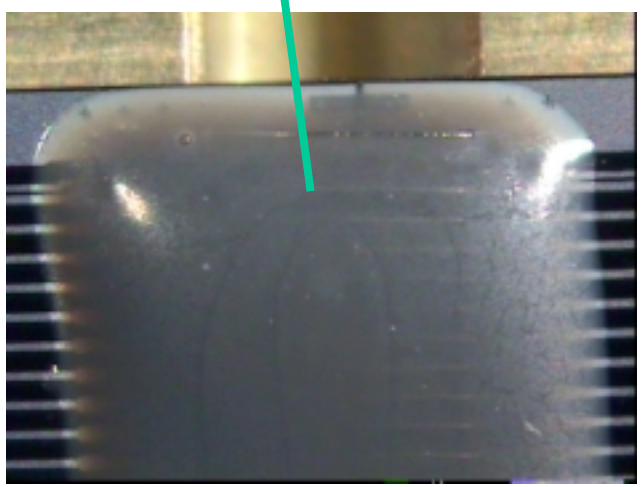
648

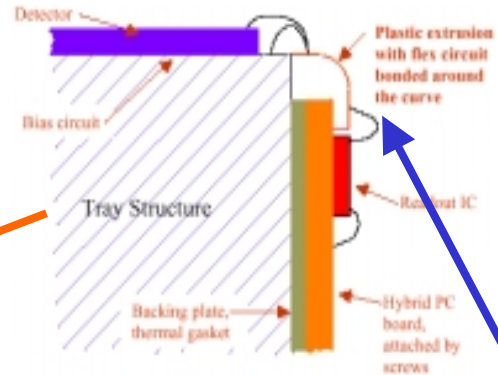
TKR Interconnects: Duck Soup?

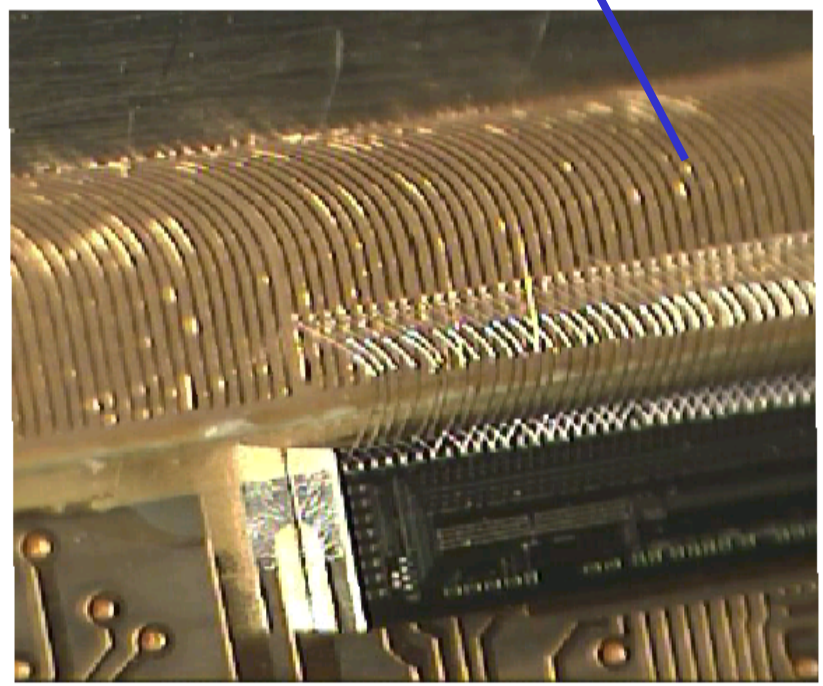
~ 1,000,000 TKR Channels

~ 6,000,000 encapsulated Wire Bonds

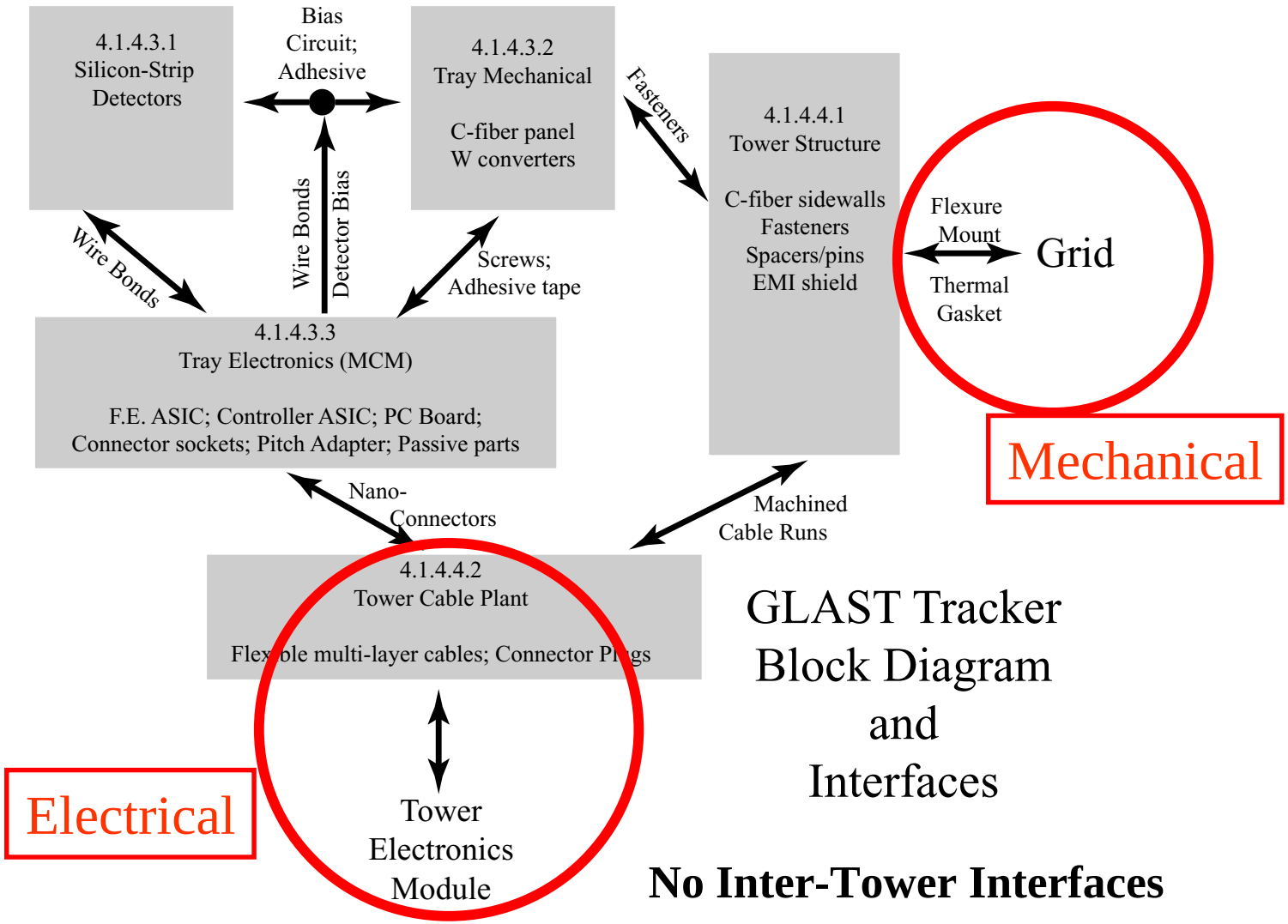








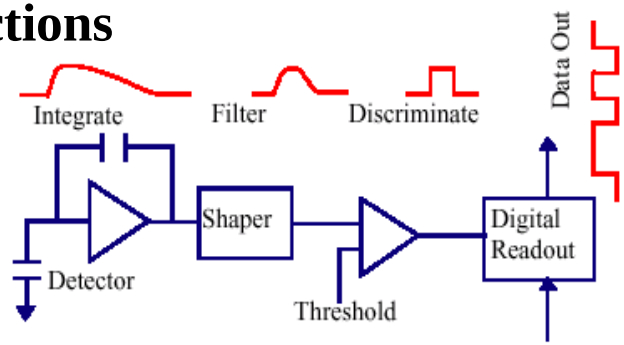
Few Clean Interfaces, No Cross strapping



SCIPP

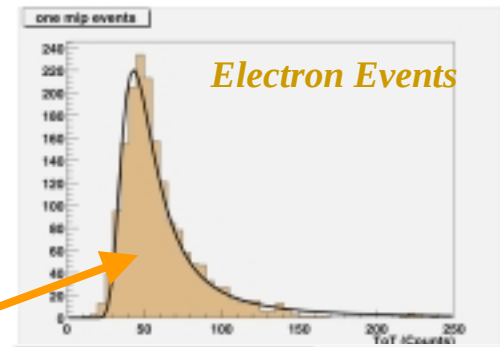
West Coast Front-End Electronics

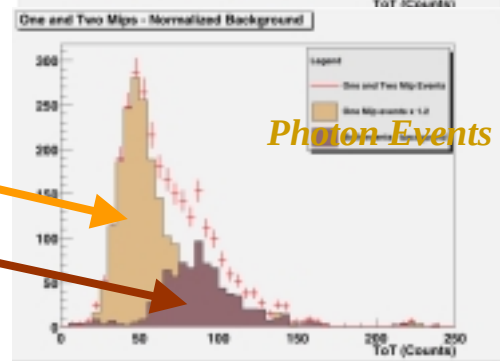
Philosophy:
get into the digital world on-chip asap
use mature engineering instead of software corrections



Binary Readout:
Low-power, low noise ASIC
Peaking time 20ns –> 1μs (L, Bkgd)
Threshold settable in every ASIC
Channel Masks
Trigger = OR of one SSD or ASIC useful

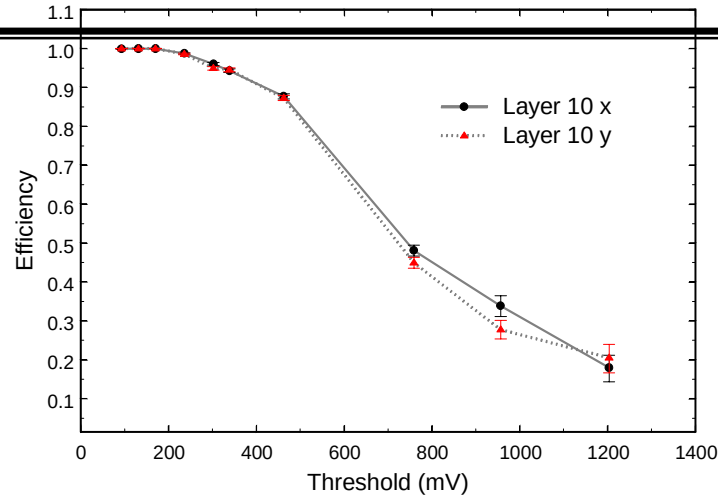
Pulse Height:
Time-over-Threshold with
large dynamic range
Distinguish single tracks
from two tracks
in one strip



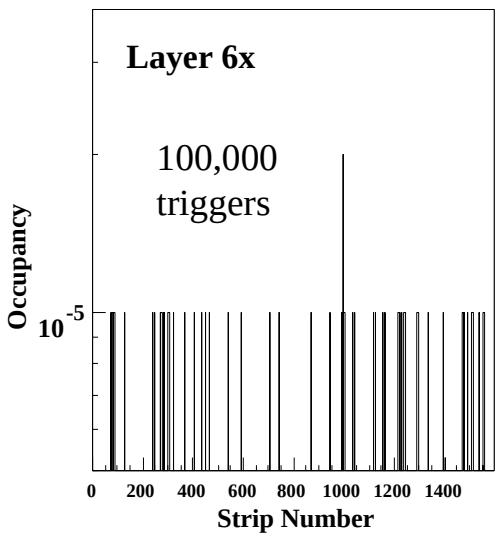


Challenge: Tracker Noise and Efficiency

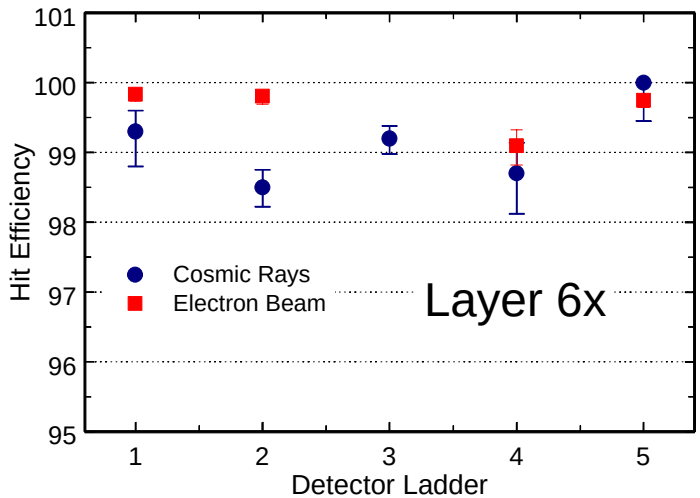
- Noise occupancy determines the noise rate of the LVL1 trigger, a coincidence of 6 OR'd layers.
- Noise RMS $\sigma = 130 + 21*C/pF\ [e^-]$, $\tau = 1.3\mu s$
- Hit efficiency was measured using single electron tracks and cosmic muons.
- The requirements were met: 99% efficiency with $<<10^{-4}$ noise occupancy.



Hit efficiency versus threshold for 5 GeV positrons.



Noise occupancy and hit efficiency for Layer 6x, using in both cases a threshold of 170 mV. No channels were masked.

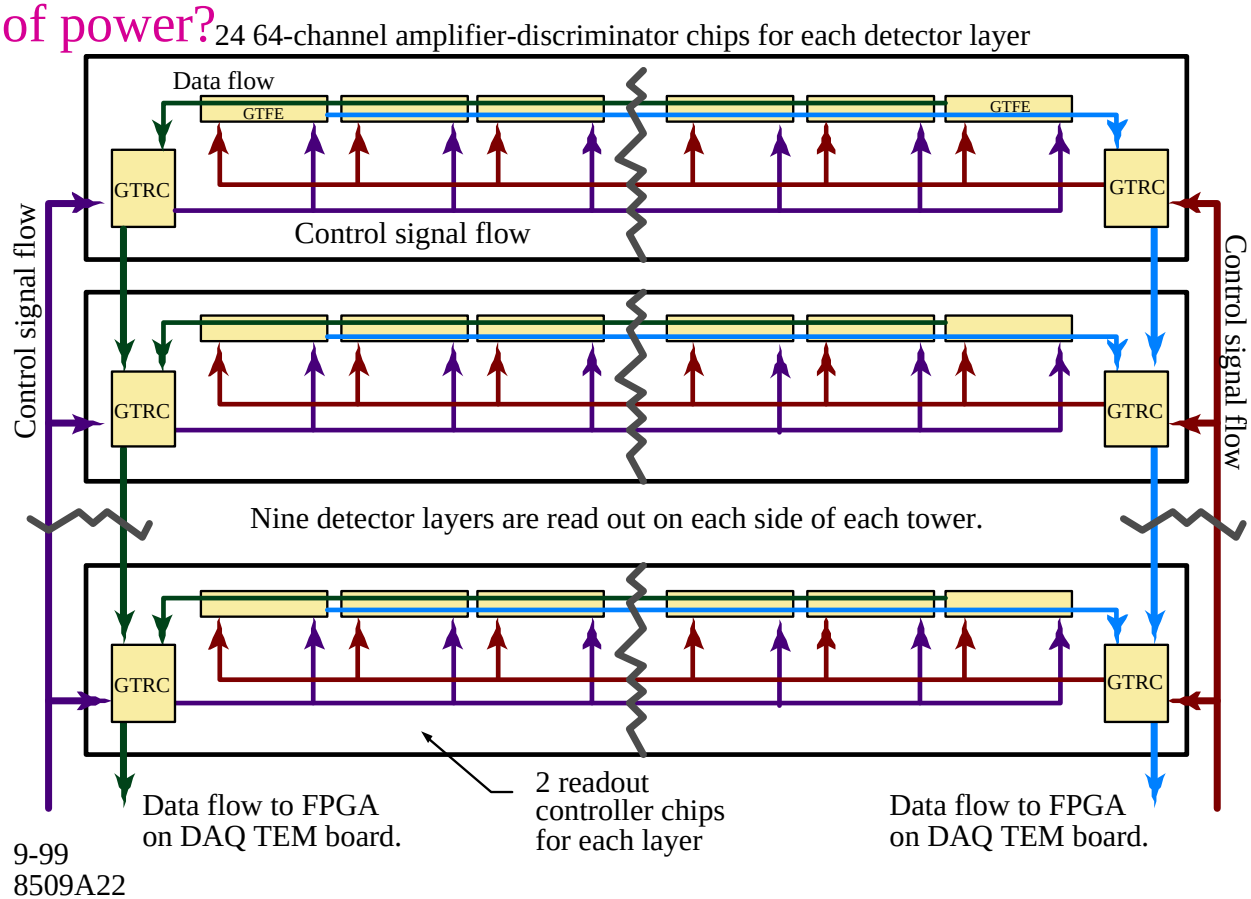


SCIPP

Redundant TKR Electronics for large Integration

- Serial, LVDS readout and control lines.
- Two readout and control paths for every 64-channel front-end chip.
- Any single chip can fail without preventing the readout of any other.
- Either of the two communications cables can fail without affecting the other.
- What about failure of power?

- Trigger output = OR of all channels in a layer.
- Upon trigger (6-fold coincidence) data are latched into a 4-event-deep buffer in each front-end chip.
- Read command moves data into the GTRC.
- Token moves data from GTRCs to TEM.



Testing/QA for the GLAST SSD: Think about Scale

Acceptance QC: flight sensors

- Order high quality SSD → testing of detectors is done by vendor:
  i-V, C-V, bad channels, R's, . NO single channel current testing!
- Measurement of parameters crucial for assembly by GLAST assembly institution:
  i-V and dimensions

Process Control: test structures

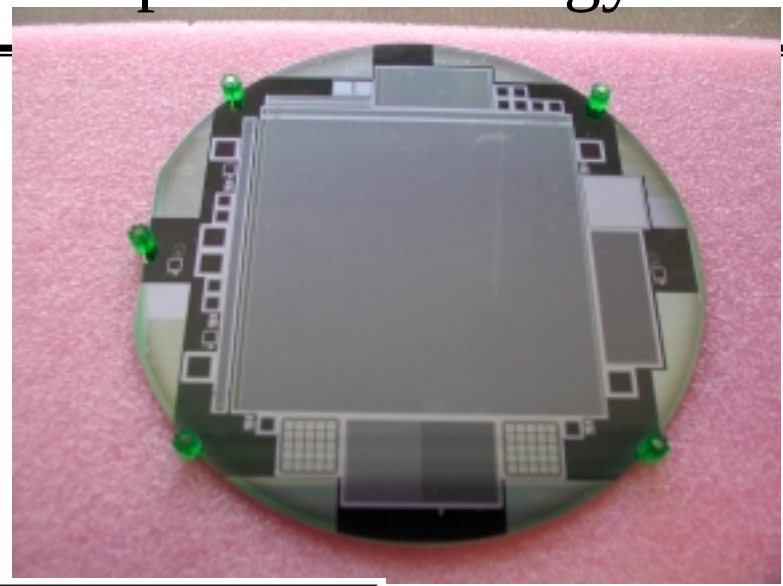
- Incorporate Test structures, test one out of every lot (48) at Hiroshima U. & INFN:
  Measure all detector parameters specified in specifications, radiation effects
- Test wire bonding and glueing on test structures

Assembly QA: flight sensors / ladders

- Testing after bonding and pre-post encapsulation by GLAST assembly institution:
  "Vital" parameters (i-V of ladders and coupling caps on every strip)
- Test before tray assembly:
  i-V on ladders

This program was based on our experience with the >500 HPK SSD in the Beam Test Engineering Module (BTEM, SLAC-8471).

GLAST SSD: Develop 6” Technology



The SSD design has been finalized and procurement is underway

11,500 SSD inlude 10% Spares/Wastage

Qualify Prototypes from HPK

(experience with ~5% of GLAST needs)

	GLAST 1996	GLAST 1997	GLAST 1998	GLAST 1999	GLAST 2000
Wafer Size	4”	4”	6”	6”	6”
Sensor Size[cmxcm]	6x6	6.4×6.4	6.4×10.7	9.5×9.5	8.95x8.95
Pitch [um]	236	194	194	208	228
Implant Width[um]	57	50	50	52	56
Thickness [um]	500	400	400	400	400
Biasing	Punch Through	Poly-Si	Poly-Si	Poly-Si	Poly-Si
Bias Voltage [V]	140	100	100	100	100
Current [nA/cm^2]		~2.5	~2.5	~1.7	~1.5
% bad strips		0.02	0.04	0.04	0.03
# delivered	~20	296	256	35	35
Use	BT’97	BTEM	BTEM	<100> Wafer	Acceptance

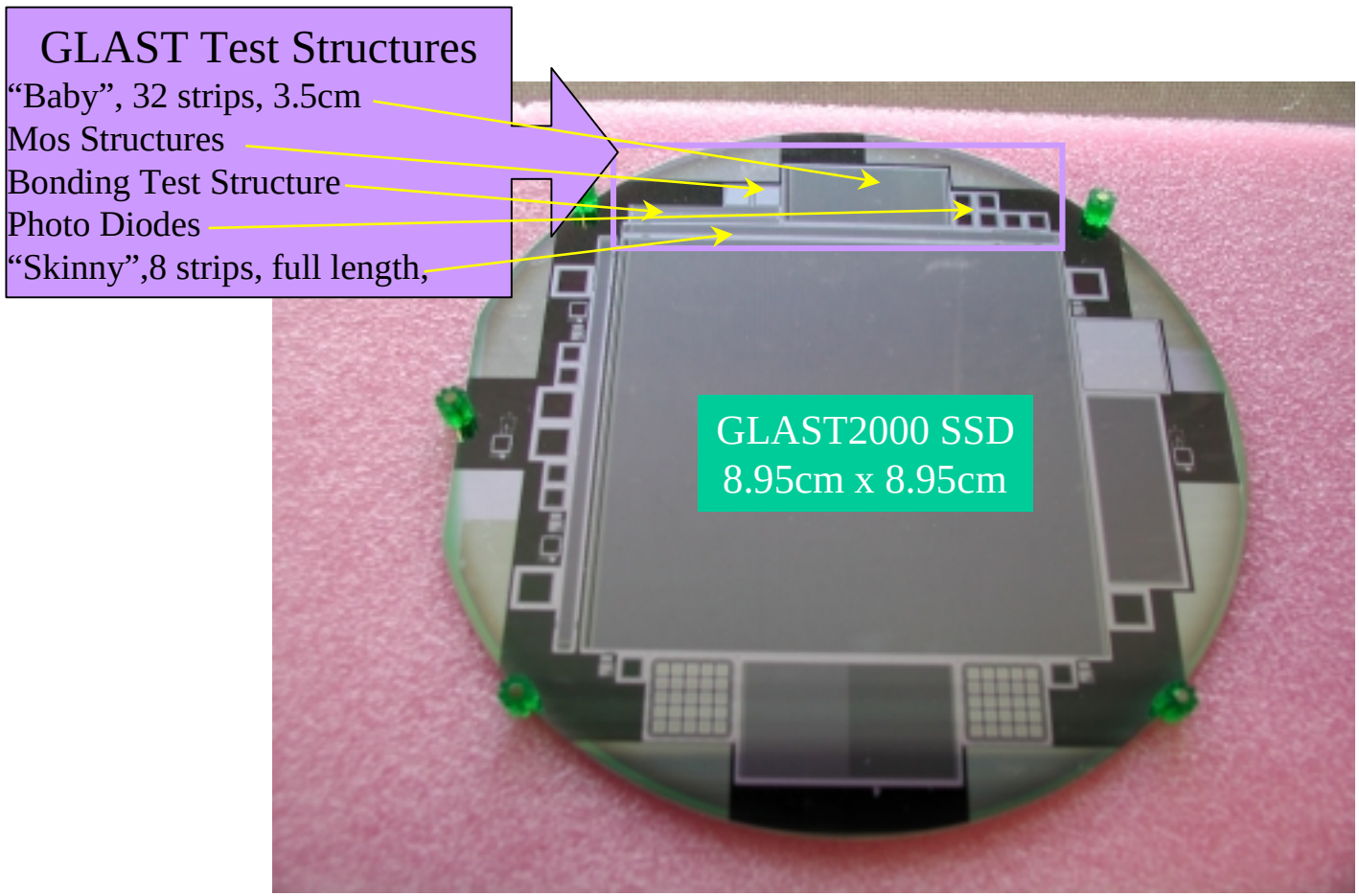
0.1*specs

+1,500

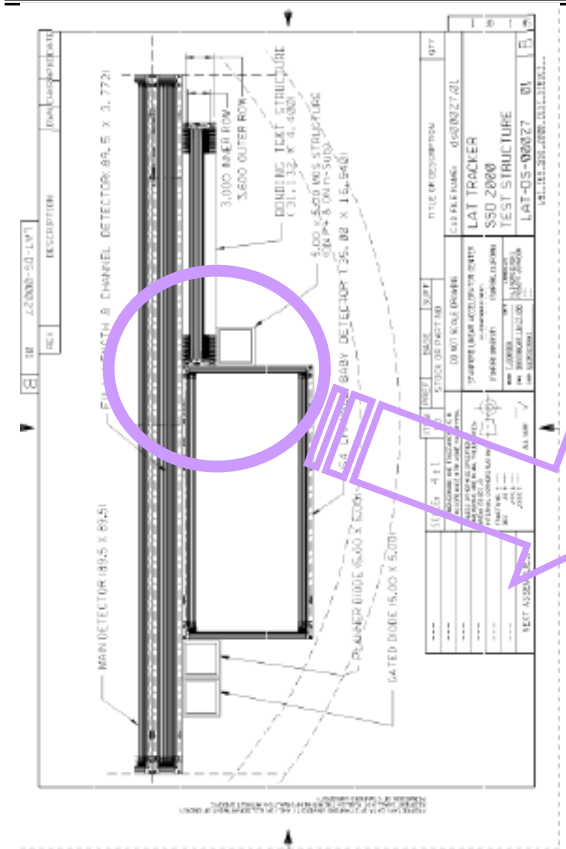
Additional Prototypes: Micron (UK), STM (Italy), CSEM (Switzerland)

6” wafer of the GLAST SSD

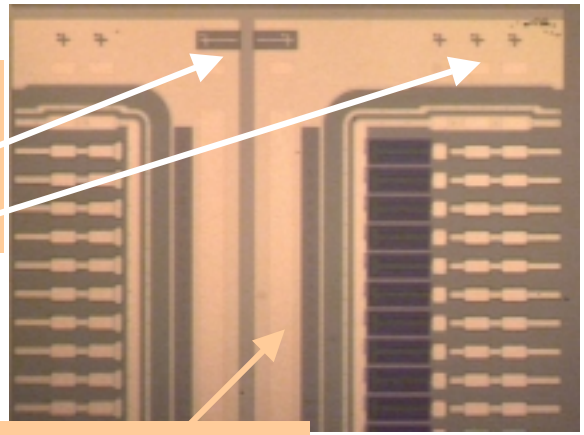
Each wafer has a GLAST2000 SSD and a GLAST cut-off.
We have established the correlation between
SSD and test structure performance.



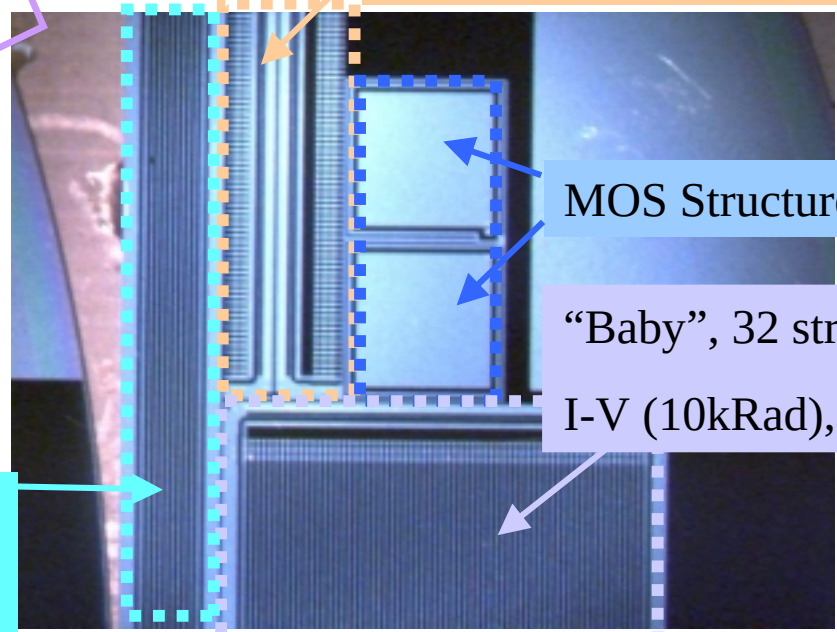
Test Structures on the GLAST SSD Wafer



Fiducials:
Alignment
Bonding



Bonding Test Structure



MOS Structures

"Baby", 32 strips, 3.5cm long

I-V (10kRad), V_{dep},

"Skinny", 8 strips, full length

C_{int}, R_{int}, R_{Al},

SCIPP

Conclusions

Finalize technical choices asap (GLAST vs ATLAS/CMS)

Choose a conservative technical solution

The cheapest solution will most likely cost you more (later)

Think big (Moore is on your side)

Think big (you will have to de-scope anyway later)

Work with Industry

Build full-size prototypes for beam tests

Adapt specifications/testing/assembly to the scale of the system

(GLAST vs. AMS)

The devil is in the services (power, cooling, DAT, …)

Do not accept a marginal solution because a strong collaborator / good friend wants it (she might not get the funding anyway)