Silicon Strip Tracking with Long Shaping Time

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USE OF SILICON STRIP DETECTORS IN LOW DUTY-CYCLE APPLICATIONS

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1 Introduction

The trend in colliding beam accelerators has been to store charge in a larger and larger fraction of the RF structure in order to maximize the luminosity during collisions. This has driven a tremendous amount of work on the development and construction of silicon-strip based detectors with fast readout for operation in such high duty-cycle environments, in order to avoid the integration of detector signals over a large number of beam crossings.

On the other hand, somewhat less attention has been paid to the low duty-cycle regime, for which one can exploit long shaping-time readout to enhance signal to noise, as well as employ power cycling to substantially reduce the complexity of the detector cooling system.

Significant research and development work has been done on long shaping-time readout in the context of astrophysical applications. Motivated largely by power budget issues, both the GLAST[1] and AMS[2] detectors employ μsec-long pulse shaping in order to permit the use of very long detector ladders, thereby substantially reducing the amount of readout electronics and servicing hardware in the detector volume.

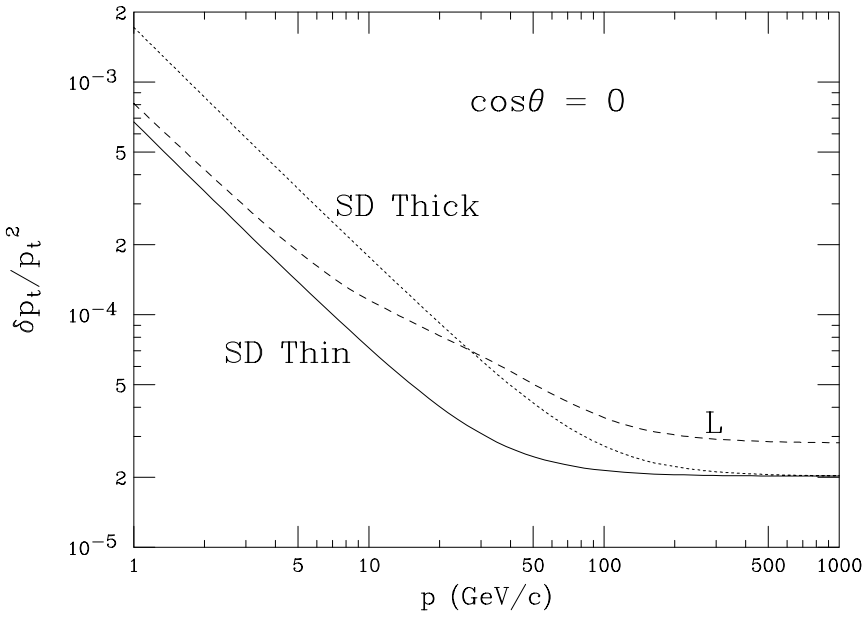
The work done by these astrophysics groups suggests that very long silicon strip detector ladders, which may well prove advantageous for use in a colliding beam environment, should be possible to construct and operate. We are proposing a program of R&D to pursue this avenue, exploring the generic issue of optimizing long shaping-time readout for operation in a low duty-cycle colliding beam environment. In addition to the advantages offered by long shaping time, the fact that the presence of colliding beams presents a triggerable signal allows for the possibility of power cycling to vastly reduce the mean I^2R power loss in the detector region.

While fairly generic in nature, these studies will be conducted with the view towards operation at a high-energy electron-positron Linear Collider in mind. The design of this machine could be that of either the US/Japan NLC or the European TESLA accelerator. The current design of the NLC machine calls for trains of approximately 200 bunches separated by 1.4 nsec each, with a train repetition rate of 120 Hz. The TESLA design calls for a 950 μs train of pulses separated by 337

Idea of the Proposal

- Long shaping time ⇒ low series (voltage-referenced) noise ⇒ long detector ladders
- Power cycling ⇒ very little power dissipation ⇒ passive cooling system

Bottom line: shoot for VERY thin detector (200 μm in three inner layers, 300 μm outer two layers) and little else.



Some Background on Noise Performance

For $> 99\%$ Landau efficiency, trigger below 1 fC (6250 e^-)

Should be x4 noise floor $\Rightarrow \sigma_{Noise} \simeq 1500\ e^-$.

Short shaping time (ATLAS CAFE chip; N = noise in e^- equiv)

$$N = 600 + 30 \cdot C$$

C = detector capacitance in pF $\simeq 1.4$ pF/cm

Limited to 20 cm ladders.

AMS 'Viking' chip:

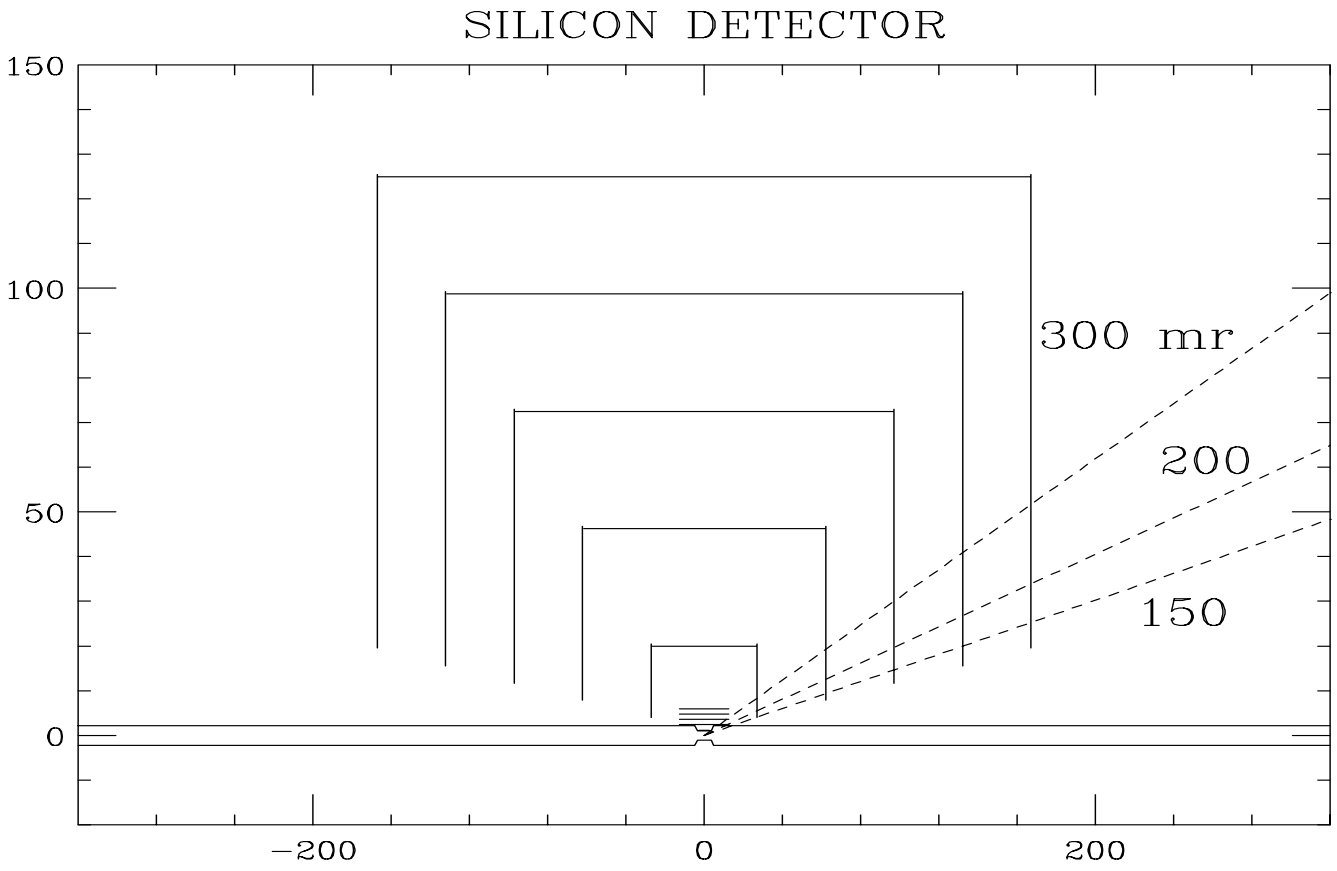
$$N = 350 + 4 \cdot C$$

suggests 2m ladders possible!

Key: Long ($\tau_S = 6\ \mu$s) shaping time stretches pulse, averaging over datector noise ($S/N \propto \sqrt{\tau_S}$)

Tradeoff: Leakage current $S/N \propto 1/\sqrt{\tau_S}$. BUT: Low radiation ($<$ 100 Rad) $\Rightarrow$ very little leakage current!

optimize


SILICON DETECTOR
150
100
50
0
−200
0
200
300 mr
200
150

Power Budget

As envisioned, SD long shaping-time tracker is 55 m^2, with just under 1 million channels.

At 100V bias, typical draw is few$\times 10^{-9}$ Amps $\Rightarrow < 0.1$W for full detector area.

At typical power use of 1 mW per channel, detector would use 1 kW at DC.

$\tau_S \simeq 10\mu$s at 100 Hz $\Rightarrow 10^{-3}$ duty cycle.

With power switching, can reduce to 1W $\Rightarrow$ very lenient instantaneous power budget! optimize

Consider: No cooling structure, minimal cabling and service (electronics at ends only) $\Rightarrow$ minimal material in endcap region.

extra material budget O(+ 2%)

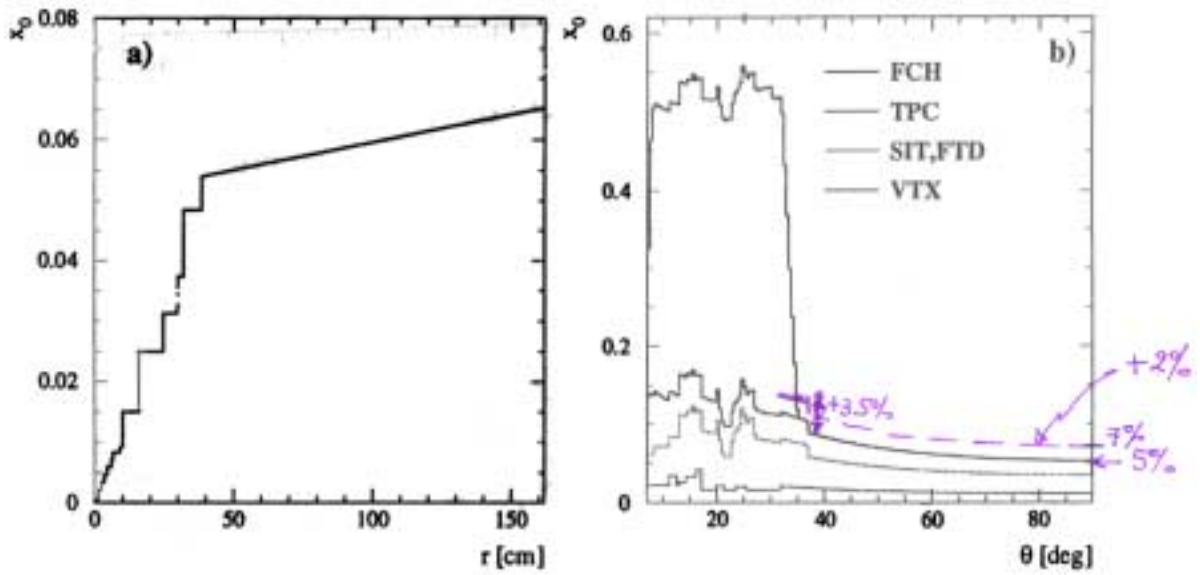
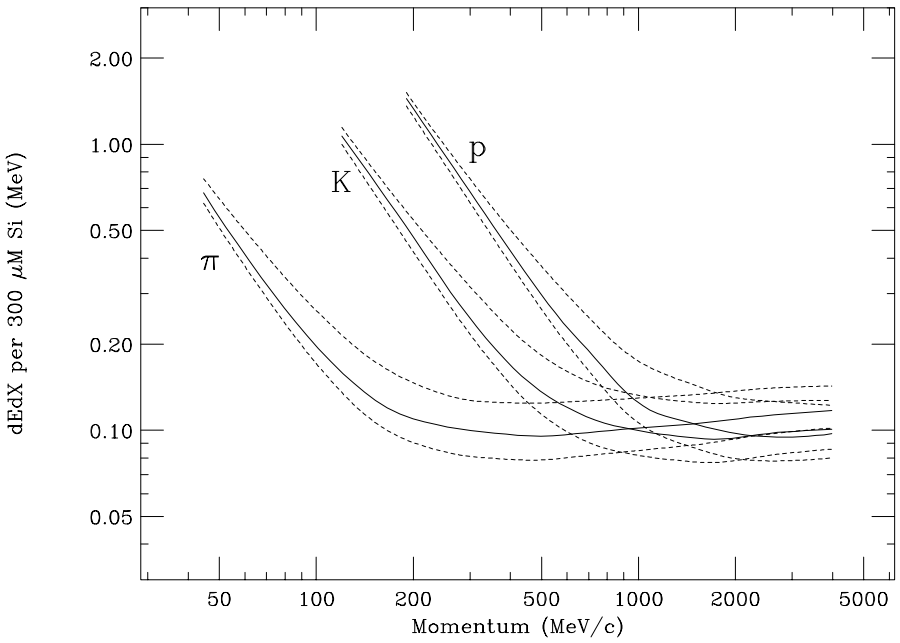


Figure 1.0.2: *Material distribution (a) as a function of the radius for $\theta = 90°$ and (b) as a function of the polar angle up to the end of the different subdetectors. For the line labelled TPC the material up to the end of the sensitive volume is shown.*

Pulse-height Issues

Intrinsic resolution of 50 μm strip $= 50/\sqrt{12} \simeq 14\mu$m. But, SD resolution assumes 7 μm $\Rightarrow$ centroid finding necessary.



Density effect limites value of Si dE/dX in min-i region. But LC interest perhaps more in $1/\beta^2$ region (long-lived exotics).

IDEA: Two-range analog readout; pulse-height to maybe $5\times$ min-i (centroid finding) and then time-over-threshold to $\sim 100\times$ min-i.

Proposed Program

6/02: Scare up grad student for studies to 1) Optimize shaping time 2) Understand dynamic range and resolution issues 3) Work with engineer (Ned Spencer) to understand realistic duty-cycle gain

9/02: Begin ASIC design (Spencer); funded by SCIPP base program (leverage!) Optimize for long, thin ladders at LC with (hopefully) generous power budget. Process: TSMC 0.25 μm mixed-signal/RF.

9/02: Begin mechanical assembly of modular long ladder (detectors exist from GLAST prototyping)

3/03: Submit ASIC

5/03: Stand-alone ASIC tests

7/03: Test ASIC in combination with ladder; irradiate (local ^{60}CO source).

Beyond (not in proposal): test beam studies

Budget

ASIC Engineering	FREE!
Ladder Detectors	FREE!
ASIC Fab (MOSIS)	$24,000
1 Yr Grad Student	$38,000
Ladder eng.	$12,000
Test board eng. and fab	$12,000
Misc. M&S	$8,000
Total (2 yrs)	$94,000

NOTE: Includes all indirect costs.

Marginal cost of making new chip (rather than testing AMS chip) is about $25K.

Conclusions

I think long shaping-time option looks very attractive *on paper*

- Performance quite similar to TPC
- Endcap-region material may be real advantage
- May be very background tolerant

WE NEED A CONCRETE PROOF OF PRINCIPLE

We also need to continue detailed simulation studies: few-layer, azimuthal-only tracking, no dE/dX in min-i region, background degradation studies.

Will talk with Aurore Savoy-Navarro (Paris) on Wednesday for possible collaboration. Some activity at UCSC (Arian Solberg, eventual undergrad thesis student), should pick up