LCD Calorimeter: Proposed Next Steps

Ray Frey, U. of Oregon, Oct 2, 2001

Summary from Sept 18 talk:

- A general-purpose LC detector *will* use EFlow.
- Question: Where on the spectrum?
  - ↓ "wimpy" (Aleph-like, $\sim 80\%/\sqrt{E_{\text{jet}}}$)
  - ↑ "extreme" (W/Si with $\lesssim 1$ cm seg [and "digital" HCal], $\sim 30\%/\sqrt{E_{\text{jet}}}$)
- We should coordinate our efforts (*if any*) internationally

Principles:

- Let's aim for the best (within loose fiscal and practical constraints) and retreat only when required to do so.
- Let's assume that a Si/W ECal is *it*.
- We should know what compromise means, both in terms of physics performance, and detector parameters and detector technologies.

Critical R&D

- Hardware: Integration of Si detectors and readout.
  - ≫ Related: Cost of detectors; gap size; transverse seg.; dynamic range
  - ≫ Not so far given sufficient weight
  - ≫ Probably *the* make/break issue for a W/Si ECal
- Software: Develop reconstruction tools.
  - ≫ Basic pattern recog.: Clustering, cal. tracking, merging, etc.
  - ≫ Combined ECal and HCal
  - ≫ Coordinate areas of emphasis with international partners

Key points (2)

Front-end with performances of a Calorimeter with the density of a tracker electronics

- **Operating during 1 ms / 200 ms[a]**
  - ⇛ **allows operation w/ active and idle mode**
  - ⇛ **power saver**
- **Two technologies investigated**
  - ⇛ **Bi-CMOS 0.8μ**
  - ⇛ **SiGe**
- **Multi-gain**

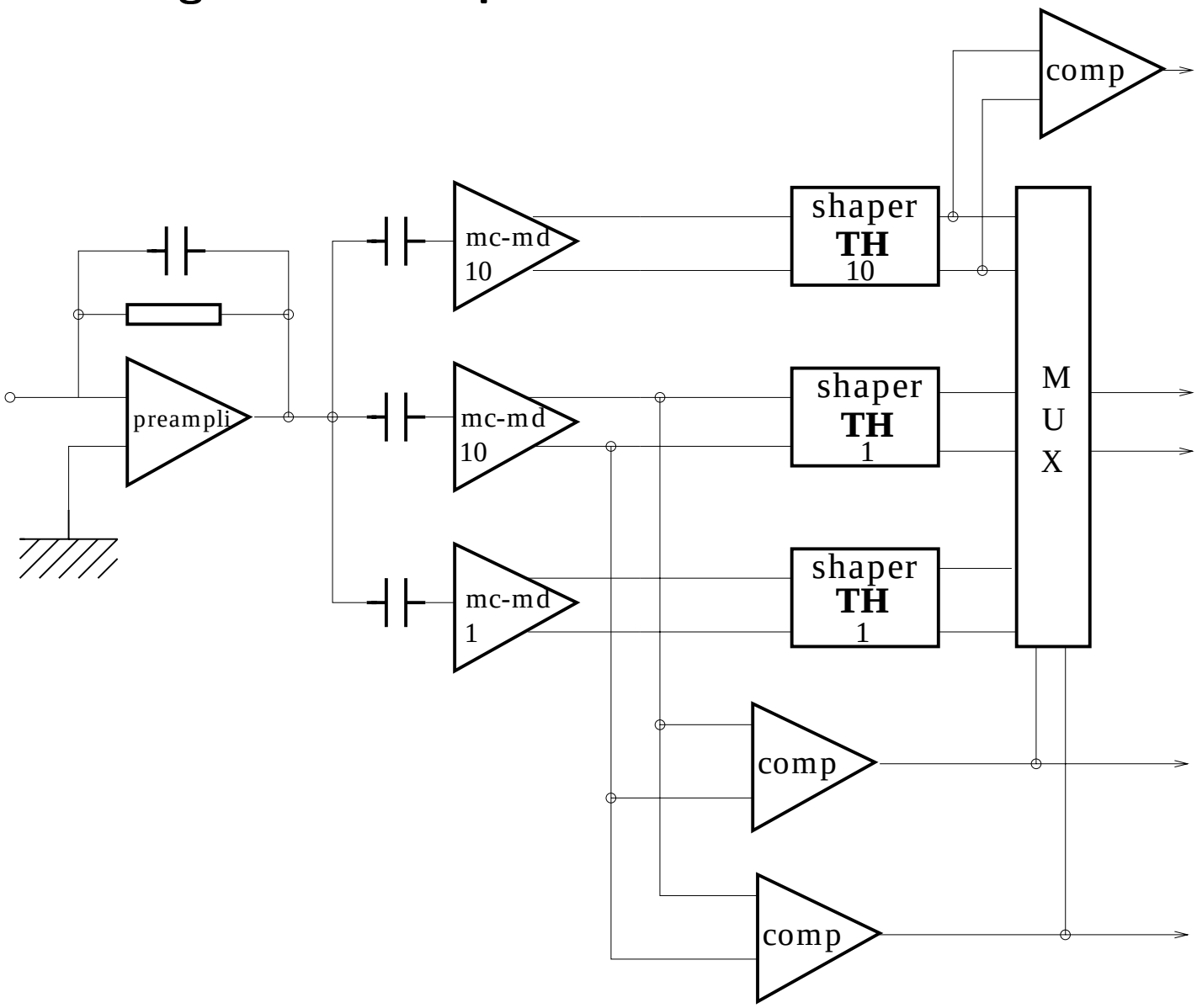
  4? more ?
- **Starting point from actual projects**

  OPERA (LAL) *Preampli*

  LHCb (LPC) *Shaper*

[a)] **beam is arranged in 3000 bunches during 1 ms every 200 ms**

First stages of the Chip



– here three gains (1, 10 and 100) which allows the full coverage, the number of gain could be increased in the future;
– zero suppress on the highest gain;

– the memory part is under investigation/studies among the three possibilities (full numeric, analogic or mixed);

Status

- **SiGe technology[a] :**

- The modelisation has been checked through a design of an amplifier

- The simulation is working, the whole chain has been checked from simulation up to real chip (test will be performed since the delivery from fonder)

- Provide an excellent Benchmark about the performances of this technology

- **Bi-CMOS 0.8μ :**

- First stage of the chip (*previously shown*) is in preparation, submission to fonder during November '01 (AMS)

- Followed by the tests

- First attempt with one channel

- Followed by a next step with 16 channels

- **Open the possibility to use it on the Physics prototype**

- **During the meanwhile, investigation/studies on design of the memory part**

a) **to be more present on the future market**

- Identify the HCal

  ≫ Digital *vs* "coarse" segmentation

  ≫ Tech. for digital (Grannis: Why not LAr?)

- Physics Simulations

  ≫ W/Z→ jets id.: quantify the benefits

  ≫ Other benchmarks (Rare: hhZ, ...; Not: SUSY, top, ...)

Also: Id./develop alternatives to Si/W for ECal – (a) coarse seg. (b) a viable fine seg. alternative?