Vertex Detectors for the Linear Collider

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Physics Opportunities of the Linear Collider

- Premier physics goals of linear collider characterized by heavy-quark decays and small cross sections
  - eg.

    Higgs branching ratios

    $t\bar{t}$ (usually 6 jets, 2 b)

    $t\bar{t}h$ (usually 8 jets, 4 b jets)

    AH (12 jets with 4 b jets)

    and other reactions

Requirements of the Vertex Detector

- Highly efficient and pure b and c tagging, including tertiary vertices ($b \to c$)
- Charge tagging (eg. $b/\bar{b}$ discrimination)
- These goals are achieved by optimized impact parameter performance:
  - point resolution < 4 μm
  - detector thickness < 0.2% X_0
  - inner radius < 2 - 3 cm
  - good central tracker linking
- Also must take care with timing and radiation hardness

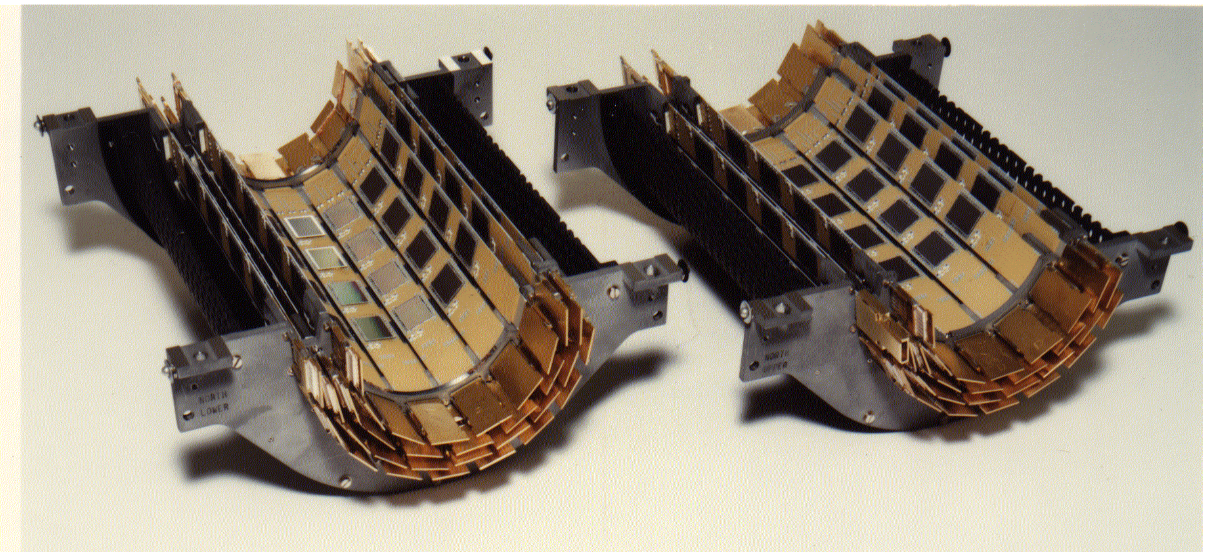
SLD has demonstrated the power of a PIXEL detector in the LC environment

- 307,000,000 pixels
- 3.8 μm point resolution
- pure and efficient flavor tagging at the Z-pole
  - ~ 60% b eff with 98% purity
  - > 20% c eff with ~ 60% purity

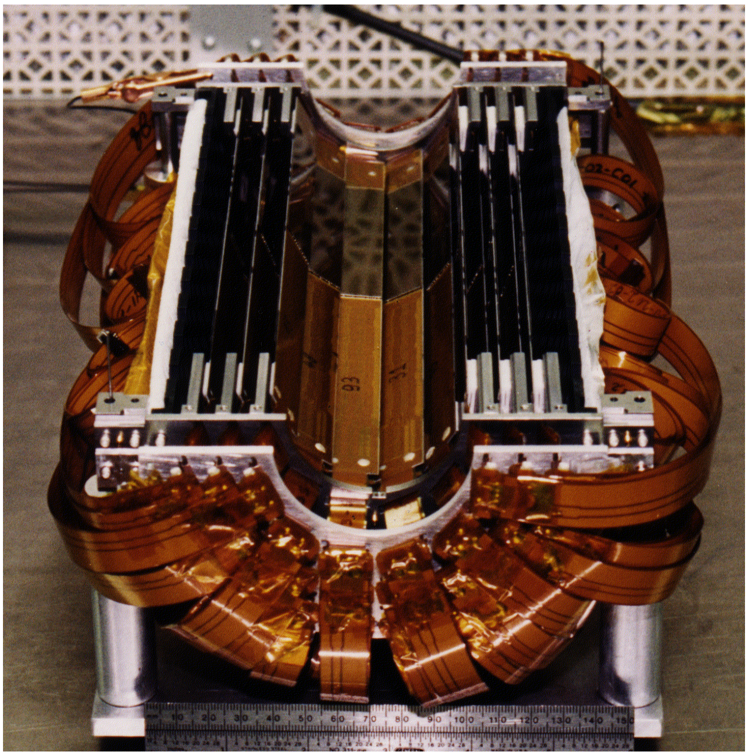
- We need a pixel solution
  - decision on option can wait
  - optimize options based on active R&D program

The SLD Vertex Detectors

VXD2 Proc 26th Int Conf on HEP, Dallas TX (1992)



VXD3 NIM A400 (1997) 287



Options under development

- CCDs
  - system level demonstration with SLD (307,000,000 pixels)
  - R&D to advance performance
- Hybrid Active Pixels (HAPDs)
  - fast, rad-hard
- Monolithic APDs
  - fast, rad-hard

We need to pursue all of these options vigorously to ensure the best possible vertex detection at the LC

D3: Vertex Detectors

Session D3

- CCDs
  - C. Damerell (system development)
  - K. Stefanov (mech./ rad-hard devel.)

- Hybrid APDs
  - M. Caccia (prototype, charge sharing)
  - G. Alimonti (“3-D” detectors, bmp bnd)

- Monolithic APDs
  - G. Deptuch (prototype, beam test)

- Performance studies
  - T. Abe (heavy jet tagging)
  - J. Brau (Higgs BRs)
  - S. Xella (flavor tagging)
  - B. Schumm (aggressive scenarios)
  - M. Battaglia (3 Tev - CLIC)
  - A. Miyamoto (flavor tagging)

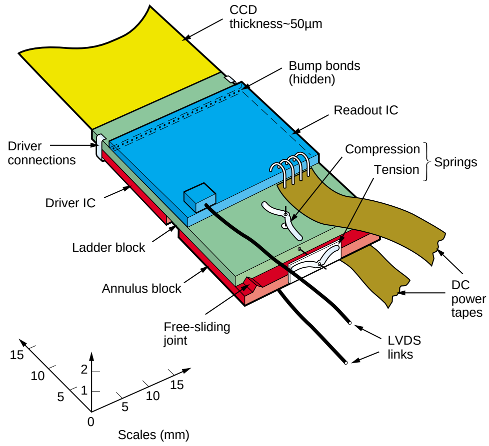
Charge Coupled Devices (CCDs)

- Chris Damerell
  - system development
    - build on SLD experience with years of operation with 307,000,000 pixels
  - 5 barrel, 799,000,000 pixels with beampipe radius of 14 mm and 3 hit coverage to cos θ = 0.96
  - thinning ladders to 0.06% X_0
  - Readout architecture
    - column-parallel readout for TESLA

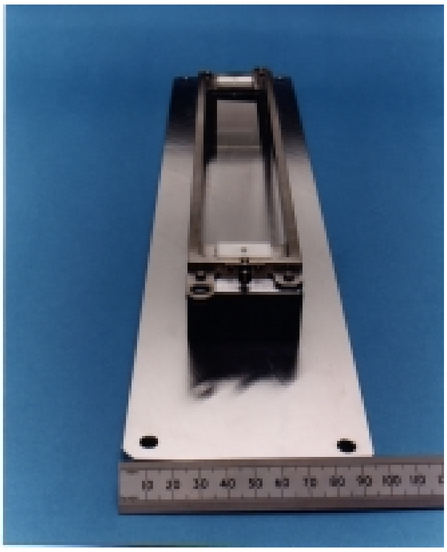
- Konstantine Stefanov
  - investigating near T_{room} use
  - mechanical design studies
  - rad-hard devel. to reduce CTI
    - improves 60-100 times
    - “will survive 10 years”

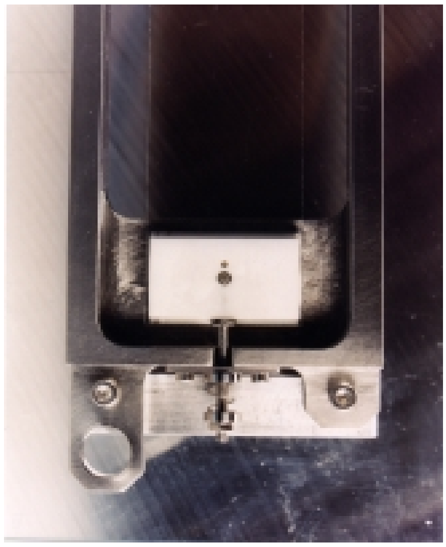
Layer Thickness

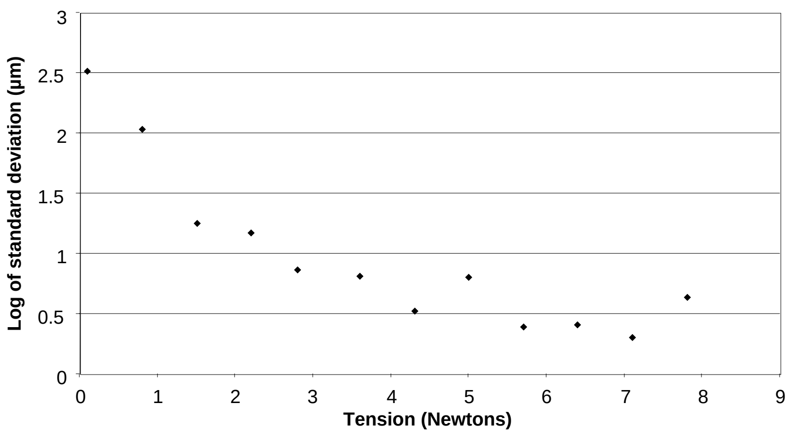
- Currently pushing the ‘unsupported silicon’ option



- Results with thin glass CCD models are most encouraging







- Assisted by the strong technology evolving for PTPs (paper-thin packages)

Readout Rate/CCD Architecture

NLC: $190 \times 120 = 22.8 \times 10^3$ bunches/s

TESLA: $2820 \times 5 = 14.1 \times 10^3$ bunches/s

Luminosity and background per bunch are similar.

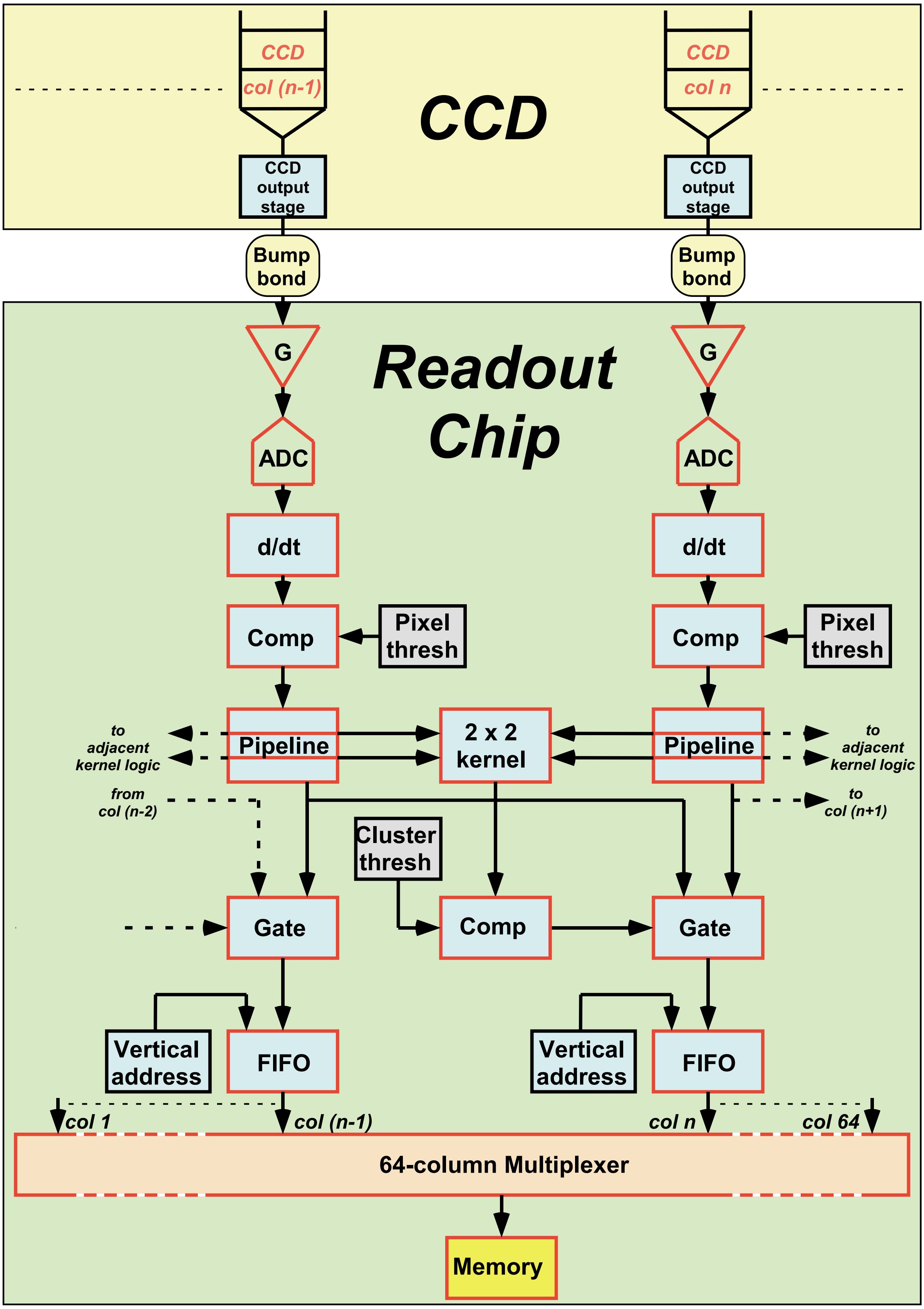
NLC: CCD readout in 8 ms between bunch trains provides adequate background control

TESLA: 15 times more luminosity per train, so need to read repeatedly during each train of 950 μs

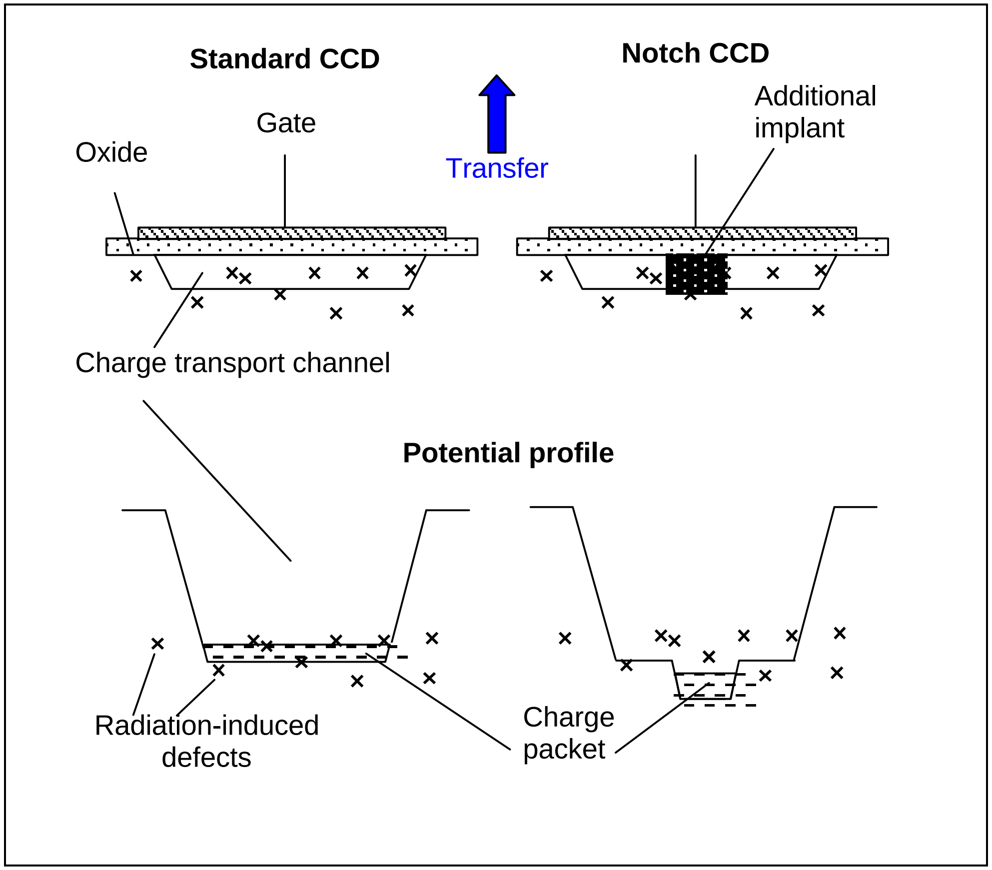
$\rightarrow$ Concept of column-parallel readout in 50 μs, which is interesting for other CCD application areas.

[An earlier option of fast clear, fast trigger and kicker magnet to kill the bgd was excluded by GMSB and other subtle signatures: the LC DAQ *must* run in an untriggered mode.]

Readout IC


CCD
CCD
col (n-1)
CCD
col n
CCD output stage
CCD output stage
Bump bond
Bump bond
Readout Chip
G
G
ADC
ADC
d/dt
d/dt
Comp
Pixel thresh
Comp
Pixel thresh
to adjacent kernel logic
Pipeline
2 x 2 kernel
Pipeline
to adjacent kernel logic
from col (n-2)
to col (n+1)
Cluster thresh
Gate
Comp
Gate
Vertical address
FIFO
Vertical address
FIFO
col 1
col (n-1)
col n
col 64
64-column Multiplexer
Memory

Notch CCD



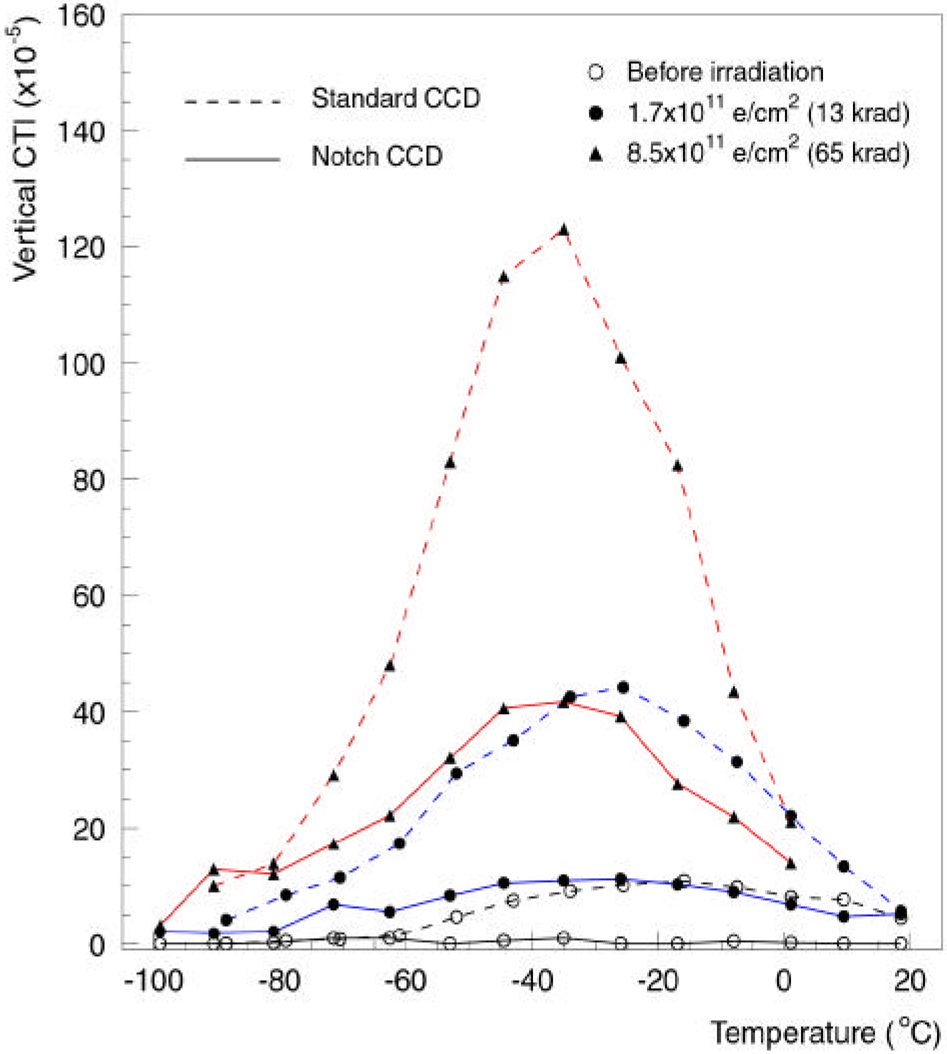
- **Additional implant in the channel;**
- **'Notch' in the potential profile;**
- **Small signal packets are transported in the notch;**
- $$\mathrm{CTI} \propto \frac{n_t}{n_s},$$

n_t **- concentration of defects,**

n_s **- concentration of signal electrons.**

Signal density for small charge packets increases

Lower CTI



Notch CCD

- **Hamamatsu Photonics Notch CCD has 3 μm wide additional implant in the channel.**

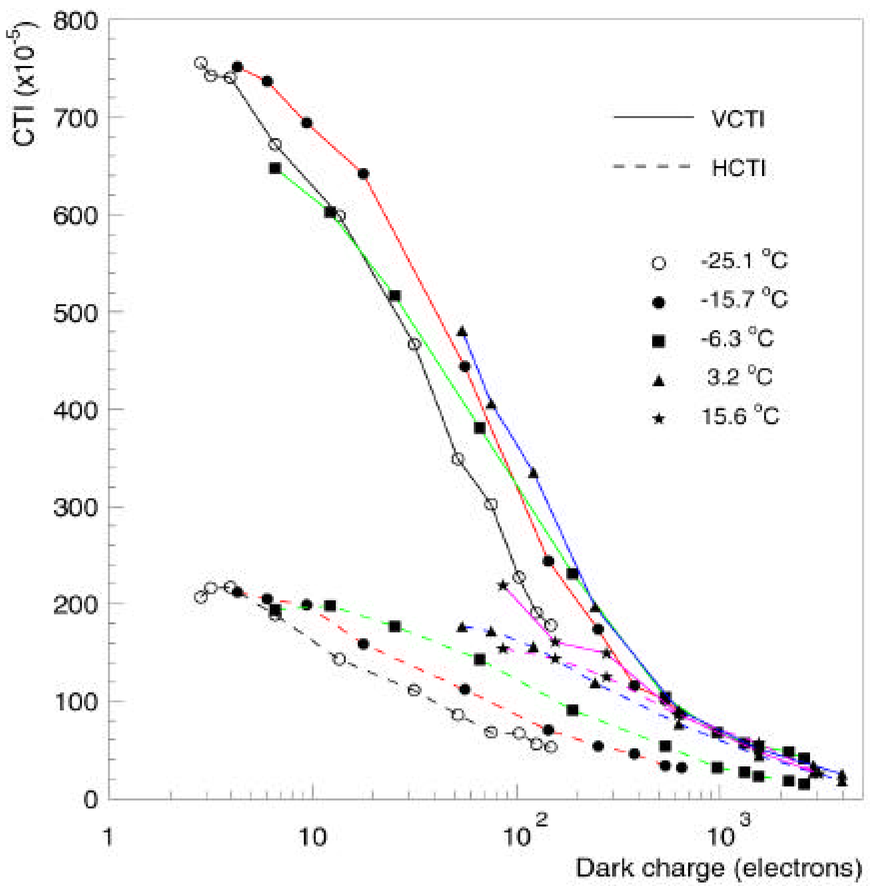
Electron irradiation:

- **Vertical (parallel) CTI is about 3 times lower than that in a conventional CCD.**

Neutron irradiation:

- **Vertical CTI of CCD, irradiated to 5.7×10^9 neutrons/cm^2 is less than 5×10^{-5}.**

Injection of additional charge (fat zero effect)



Dark current electrons occupy traps

Less signal electrons are lost

The most powerful method for reducing charge losses

- **Injection of 1000 electrons introduces 32 electrons (RMS) noise**
- **Noise of high speed CCD: about 100 electrons (RMS)**
- **Requires CCD with an injection structure**

Experiment on EEV02-06 CCD: 8 to 10 times CTI reduction

CTI improvements

After 10 years of operation ($\approx 5\times10^{12}$ electrons/cm^2 ^{90}Sr, and $\approx 5\times10^{9}$ neutrons/cm^2 ^{252}Cf)

- **Vertical CTI reaches 4.8×10^{-2} (at maximum, 250 kpix/s)**
- **Horizontal CTI is much smaller than the VCTI.**
- **Neutron irradiation causes small CTI.**

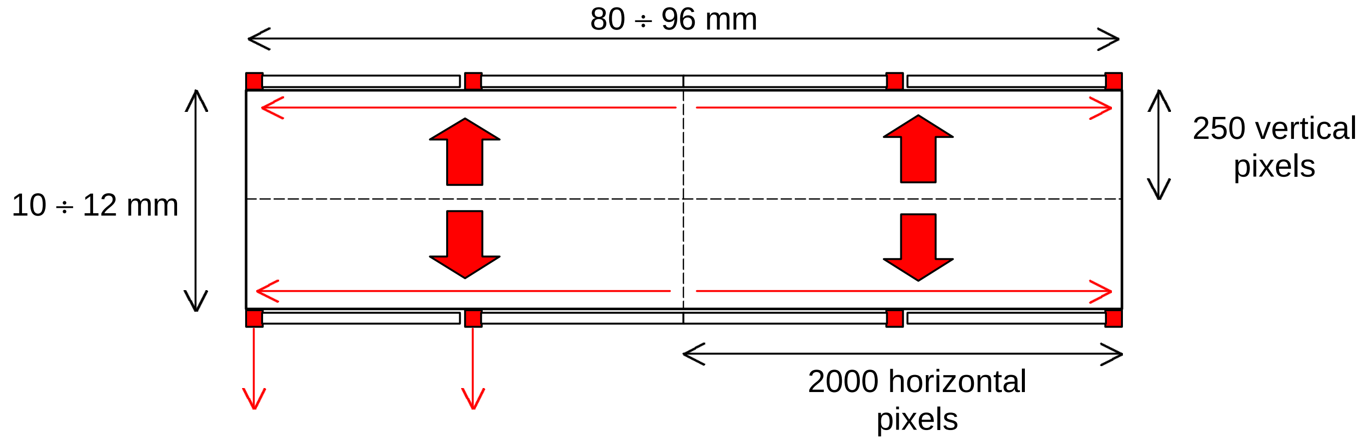
Budget for improvement:

Option	VCTI improvement
Raise the readout speed to > 5 Mpix/s	≈1.3 times
Use 2-phase CCD	≈2.5 times
Use notch CCD	3 to 4 times
Inject dark charge ≈1000 electrons (at >5 °C)	6 to 8 times
Total improvement :	≈ 60 to 100 times

Recent simulation gives 1.5×10^{12} e^+e^- pairs/cm^2/10 years, however their energy is higher than ^{90}Sr electrons (safety margin of 10 gives 15×10^{12} electrons/cm^2 ^{90}Sr).

Model CCD

Based on the present knowledge on radiation damage effects and device architecture



Reduced worst-case CTI:

Vertical CTI to $\approx 8\times10^{-4}$**, output charge after 250 transfers:** $(1 - 8\times10^{-4})^{250} = 0.82$ **(18% loss)**

Horizontal CTI to $\approx 8\times10^{-5}$**, output charge after 1000 transfers:** $(1 - 8\times10^{-5})^{1000} = 0.92$ **(8% loss)**

Total charge at the output: $0.82\times0.92 = 0.75$ **(25% loss)**

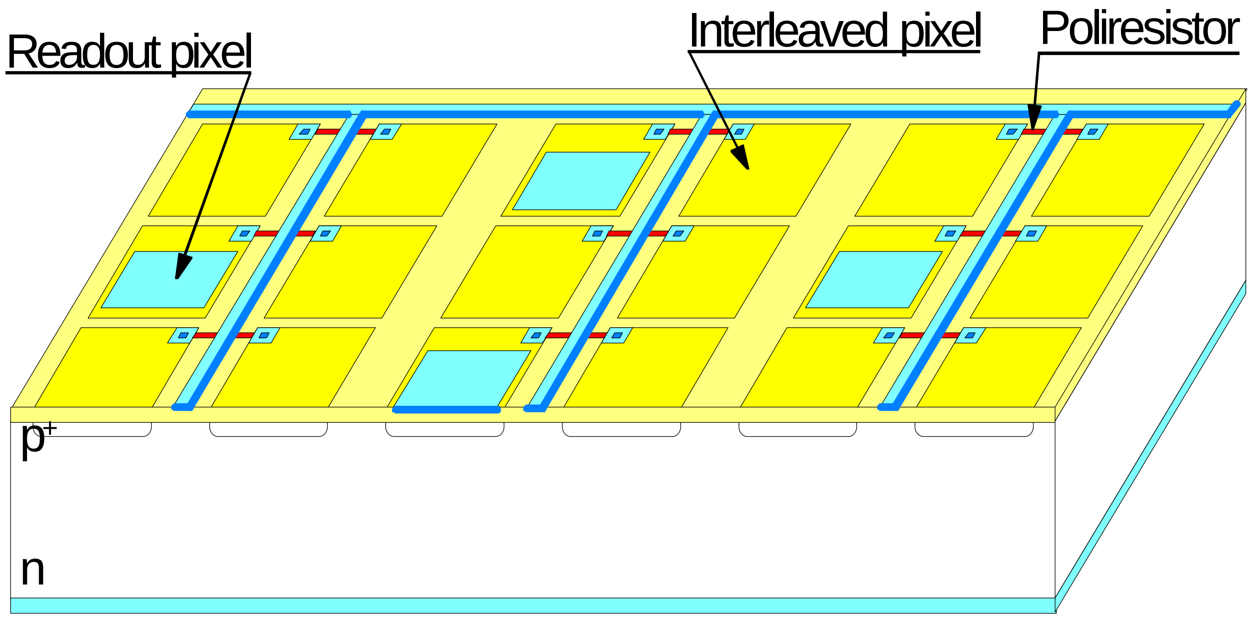
The CCD will survive for 10 years ($\approx 5\times10^{12}$ **electrons/cm^2** ^{90}**Sr,** $\approx 5\times10^{9}$ **neutrons/cm^2** ^{252}**Cf), or for 3 years (at** 15×10^{12} **electrons/cm^2)**

Hybrid APDs (Active Pixel Devices)

- Massimo Caccia
  - readout pitch > pixel pitch
  - prototype tested
  - charge sharing efficiency demonstrated
  - next step ⇒ beam test of improved device

- Gianluca Alimonti
  - first “3-D” detectors fabricated
    - leakage currents 1/4-1 nA/mm^3 (T_{room})
    - low depletion voltage
    - active edges
  - Rad-hard XTEST2
  - bump bond yields good
  - next year ⇒ prototype system

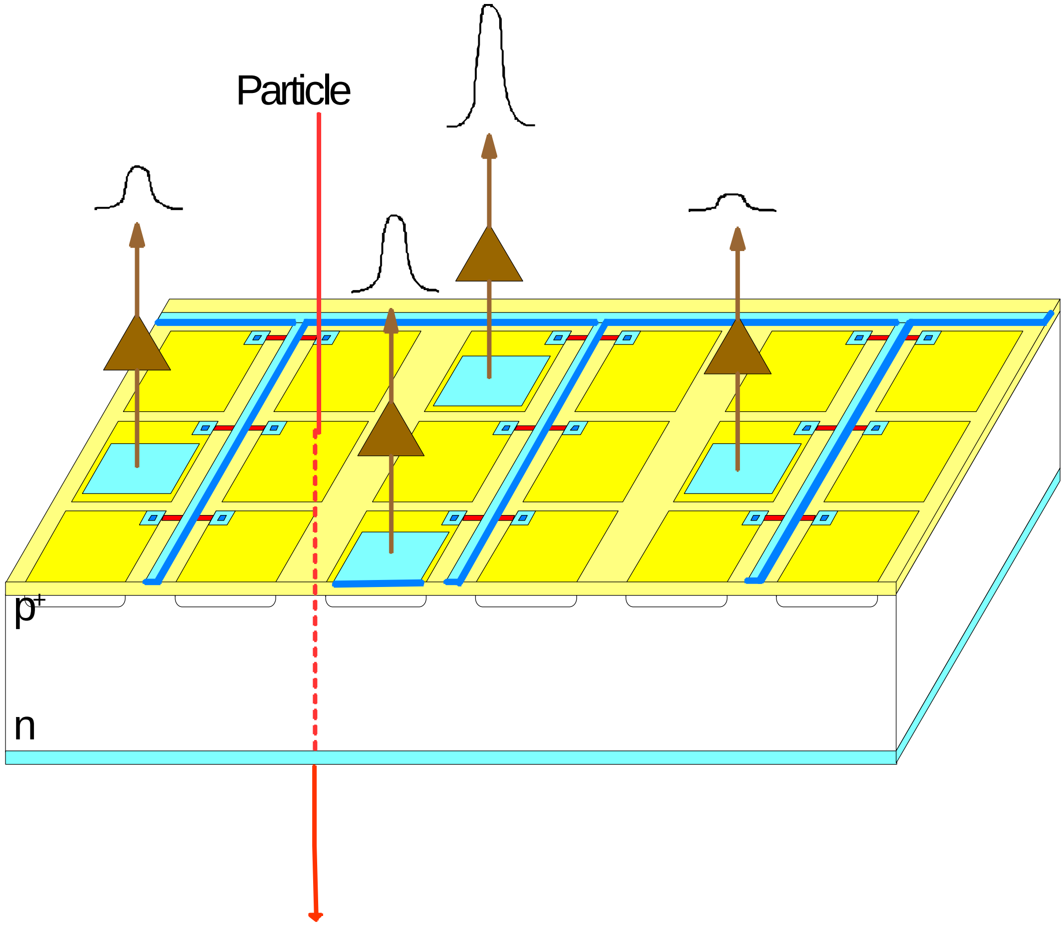
Hybrid detector with interleaved pixels between the output nodes



readout pitch = n x pixel pitch

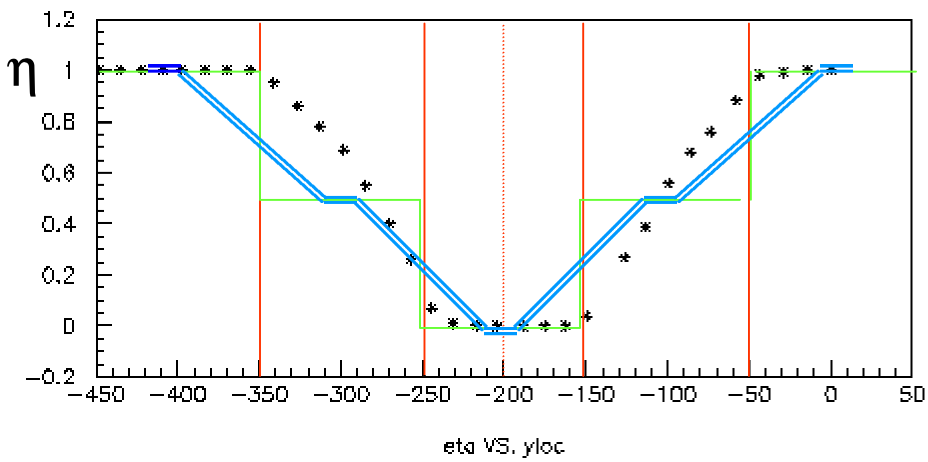
Large enough to house the VLSI front-end cell

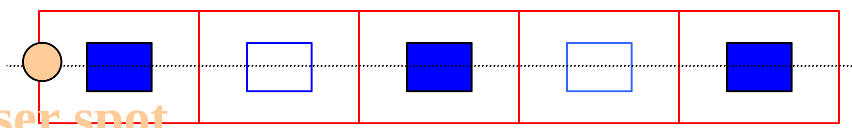
Small enough for an effective sampling



Due to the capacitive charge division a particle will induces a signal on the surrounding pixels beyond the diffusive charge carrier spread

Charge sharing II





Read out pixels

Interleaved pixels

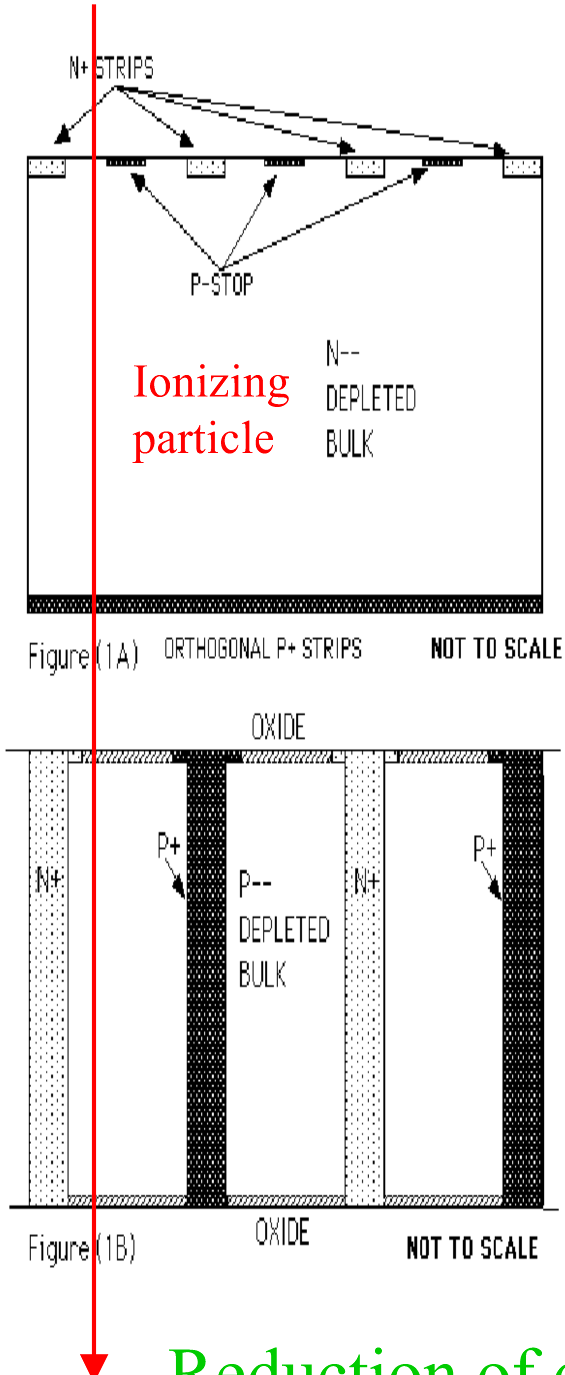
NO diffusion, capacitive coupling only

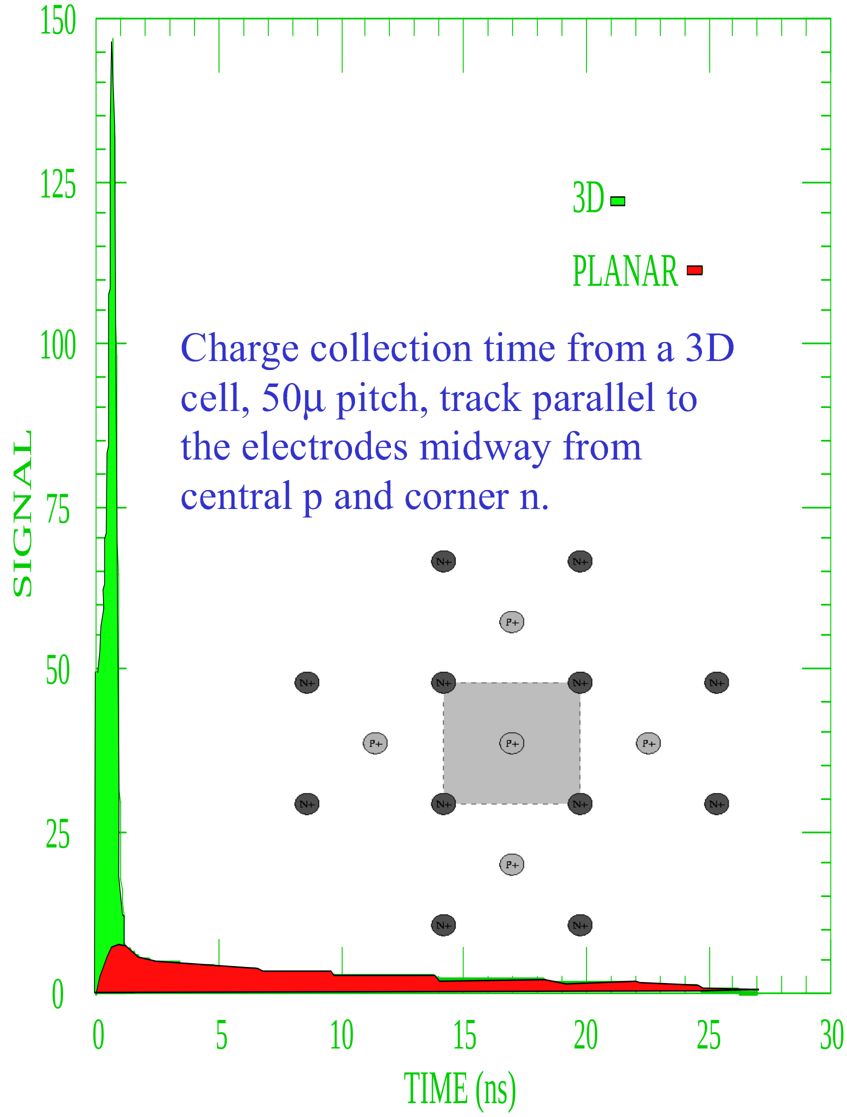
Diffusion and capacitive coupling with a 25 μm pitch

Resolution < 25 μm/√12

Detector Development

Good timing!



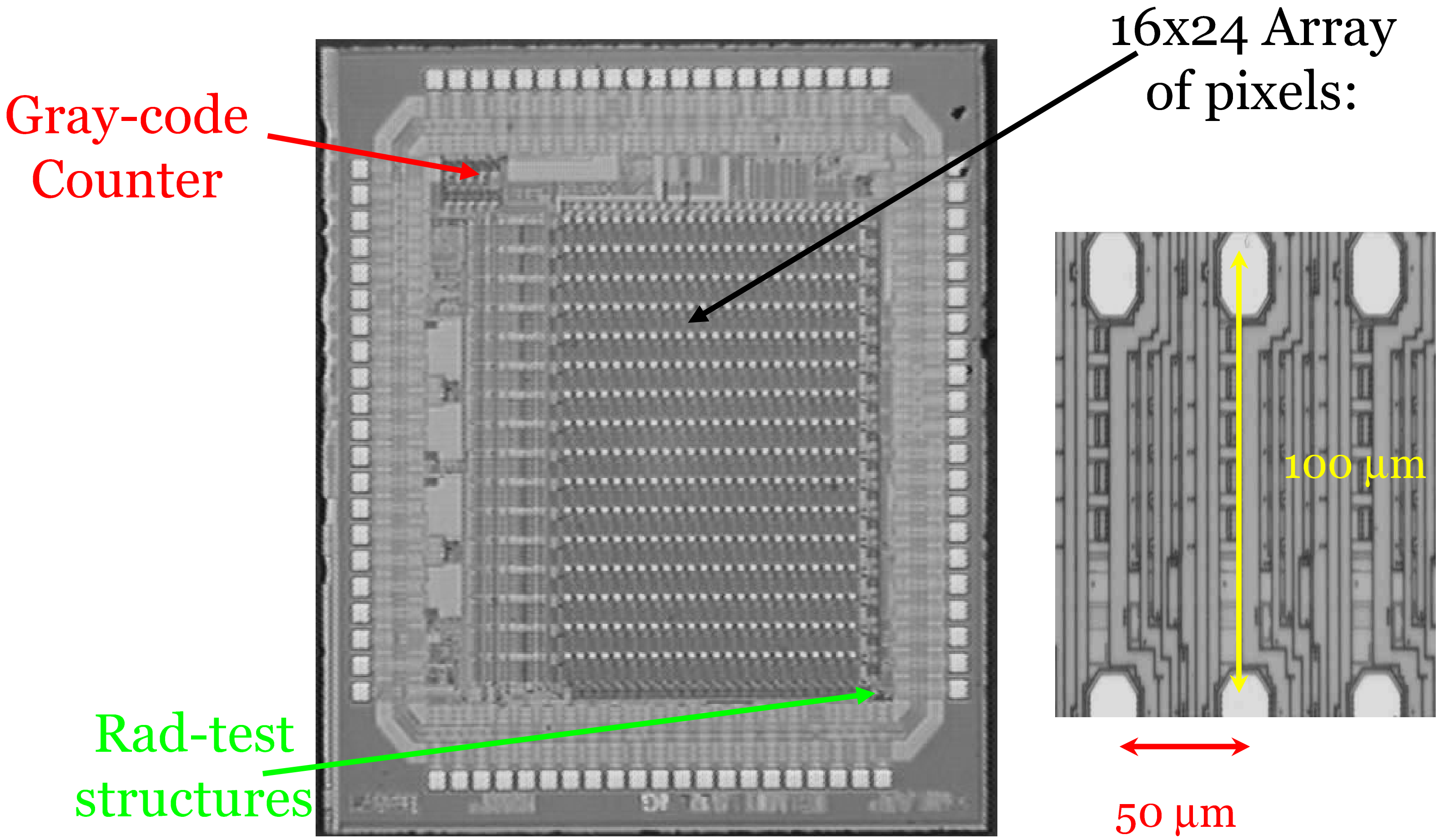


Reduction of distance between electrodes:

- Reduction of drift time
- Reduction of depletion voltage

XTEST2 Initial Prototype

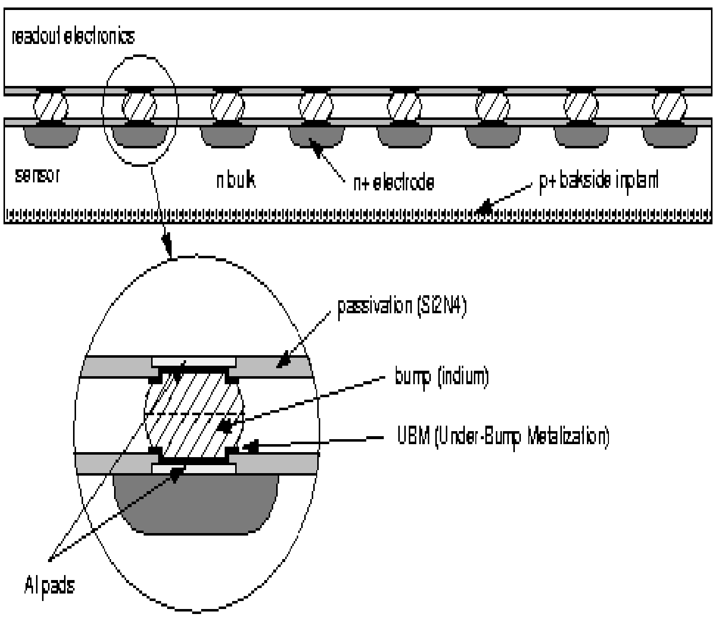
To test feasibility, a prototype (XTEST2) was fabricated in HP 0.5 µm; going to .25 µm technology it is expected to fit in 50X50 µm (or 40X60 µm)

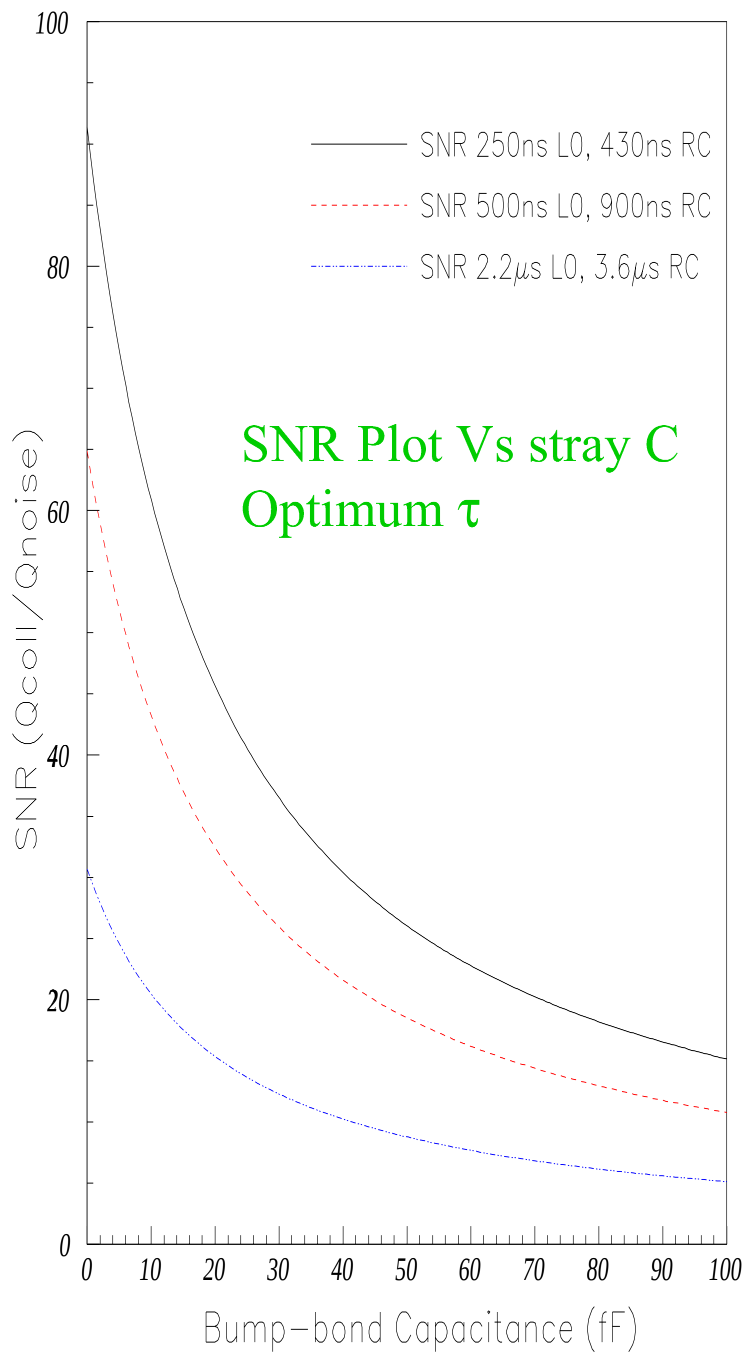


Interconnect Concerns

- Excellent SNR and Timing, but…

Assumption all charge is collected is FALSE!





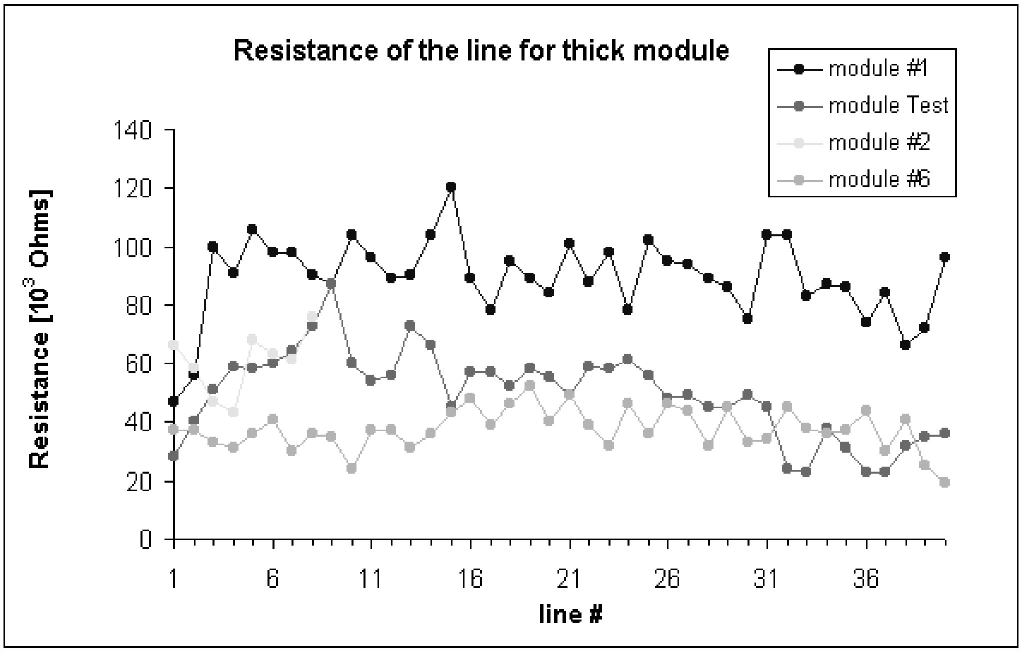
SNR Plot Vs stray C
Optimum τ

For faster trigger time, even 100fF stray C would yield to SNR about 20.

For larger stray C the degradation may become unacceptable.

Test bumps for real measurement (evaluation from first principles is quite complex)

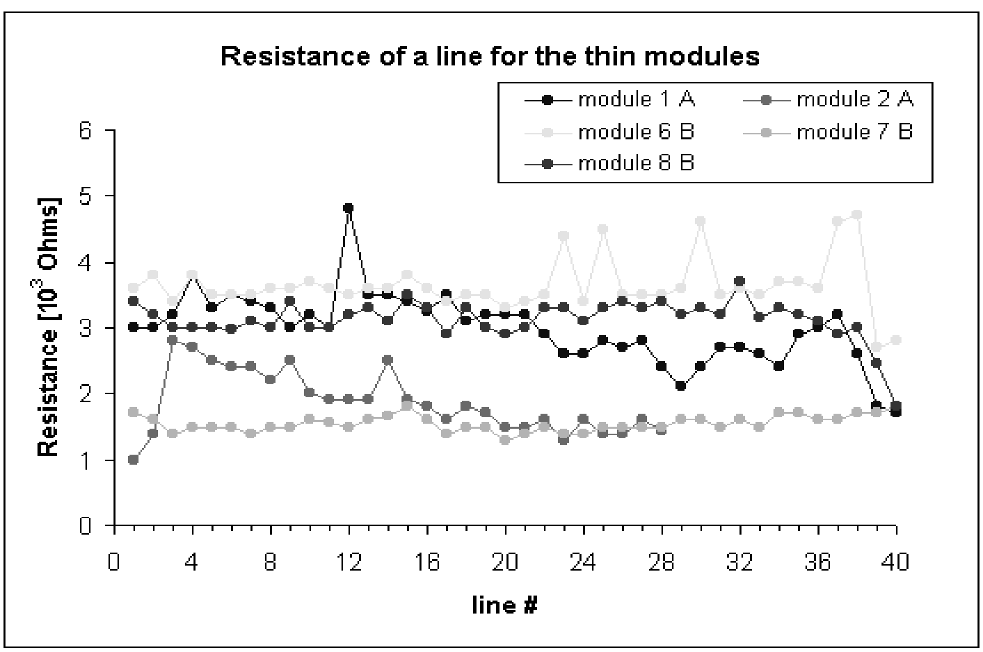
Bump bonding Results



•No open bump-to-bump connection observed out of 21120

• About 20% of chips bad (learning chips…)

•Using final "recipe", the remaining 80% had a rate of inter row shorts of about one in a thousand



Monolithic APDs (CMOS)

- G. Deptuch
  - prototype tested with beam
    - 64 x 64 pixel arrays
  - next year ⇒ increase size
    - ~ 10 cm
  - outstanding potential
    - rad-hard
    - high precision
    - ultra thin
    - low cost
  - issues to address
    - expand to system
    - power

Performance studies

- Bruce Schumm
  - aggressive scenarios (just to see)
    - improved resolution (⇒ 1 μm)
    - smaller beampipe (⇒ 0.5 cm)
    - greater radial extent (⇒ 11 cm)
    - thinner layers (and pipe) (⇒ 0.06% X_0)
  - conclusions:
    - good central tracking vital
    - spatial resolution and beampipe radius lead to substantial improvements

- Akiya Miyamoto
  - flavor tagging
  - conclusion:
    - significant improvement with inner radius of 1.2 cm vs. 2.4 cm

Performance studies

(continued)

- Toshi Abe
  - heavy jet tagging
  - ZVTOP installed into LCD simulation
- Stefania Xella
  - flavor tagging with neural net including ZVTOP
  - update for new TESLA geometry
  - future $\Rightarrow$ ZVTOP3, vertex charge, dipole charge
- Jim Brau
  - detector parameters and Higgs BRs

Performance studies

(continued)

- Marco Battaglia
  - 3 Tev - CLIC
  - extreme energies lead to some very long decay lengths (several cm)
  - proposes counting tracks with pulse height information
  - demonstrates viability with simulation of $\sigma(e^+ e^- \rightarrow b \bar{b})$ determination

Summary of LCWS2000

- Progress continues to advance on many fronts
  - CCDs
    - R&D to advance the already demonstrated exceptional system-level performance
  - Hybrid APDs
    - prototypes with charge sharing understood
    - "3-D" detectors fabricated
  - Monolithic APDs
    - effort to capitalize on industry standards
    - first chip shows extraordinary promise
  - Performance simulations
    - tradeoffs becoming clearer

Future Directions

- Continue progress on all fronts
    - CCDs
    - Hybrid APDs
    - Monolithic APDs
- Performance simulations
    - Refine our understanding of the impact of detector trade-offs on physics performance
- We will be able to exploit the exceptional physics opportunities of the LC